MASTER OF TECHNOLOGY
In
VLSI & EMBEDDED SYSTEMS

ACADEMIC REGULATIONS, COURSE COVERAGE SUMMARY
&
QUESTION BANK

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)

Sponsored by CMR Educational Society

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NAAC – 'A' Grade - ISO 9001:2015 Certified)
Maisammaguda, Dhulapally, Kompally, Secunderabad – 500100, Telangana State, India.
Contact Number: 7207034237, 9133555162, E-Mail ID: mrcet2004@gmail.com, website: www.mrcet.ac.in

Vision

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

Mission

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

Quality Policy

Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
Make the students experience the applications on quality equipment and tools.
Provide systems, resources and training opportunities to achieve continuous improvement. Maintain global standards in education, training and services.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.TECH – VLSI & EMBEDDED SYSTEMS

COURSE STRUCTURE

I Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R18D6801	VLSI Technology & Design	3	-	3	30	70
2	R18D6802	CPLD & FPGA Architectures& Applications	3	-	3	30	70
3	R18D6803	Embedded System design	3	-	3	30	70
4	R18D6807 R18D6808 R18D6809	ELECTIVE-I 1.VLSI Signal Processing 2.CMOS Analog Integrated Circuit Design 3.Programming Languages for Embedded Software	3	-	3	30	70
5	R18D6810 R18D6811 R18D6812	ELECTIVE-II 1.CMOS Digital Integrated Circuit design 2.CAD of Digital System 3.System Design with Embedded Linux	3	-	3	30	70
6	OE I	OPEN ELECTIVE –I	3	-	3	30	70
7	R18D6881	VLSI Lab	-	3	2	30	70
8	R18DHS54	Audit Course I - Value Education	2	-	-	50	-
Total			20	3	20	260	490

*Audit course: Non-credit course, 50% of scoring is required for the award of the degree

OPEN ELECTIVE I	
Subject Code	**Subject Name**
R18DME51	Non-Conventional Energy Sources
R18DME52	Industrial Safety
R18DME53	Operations Research
R18DHS51	Business Analytics
R18DCS51	Scripting Languages
R18DAE51	Mathematical Modeling Techniques
R18DEC51	Embedded Systems Programming

I Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R18D6804	Embedded Real Time Operating Systems	3	-	3	30	70
2	R18D6805	CMOS Mixed Signal Circuit Design	3	-	3	30	70
3	R18D6806	Low Power VLSI Design	3	-	3	30	70
4	R18D6813 R18D6814 R18D6815	ELECTIVE – III 1.Adhoc –Wireless Networks 2.SOC Design 3.Memory Technologies	3	-	3	30	70
5	R18D6816 R18D6817 R18D6818	ELECTIVE- IV 1.Physical Design Automation 2.Communication Buses and Interfaces 3.Multimedia Signal Coding	3	-	3	30	70
6	OE II	OPEN ELECTIVE- II	3	-	3	30	70

7	R18D6882	Embedded Systems Lab	-	3	2	30	70
8	R18DHS55	Audit Course II - English for Research Paper Writing	2	-	-	50	
Total			20	3	20	260	490

*Audit course: Non-credit course, 50% of scoring is required for the award of the degree

OPEN ELECTIVE II	
Subject Code	Subject Name
R18DME54	Composite Materials
R18DME55	Waste to Energy
R18DME56	Industrial Management
R18DHS52	Cost Management of Engineering Projects
R18DCS52	Information Security
R18DAE52	Unmanned Aerial Vehicles
R18DEC52	Research Methodology

II Year I Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R18D6883	Seminar-I	-	-	2	50	-
2	R18D6891	Mini Project	-	-	4	100	-
3	R18D6892	Project Review-I	-	-	8	100	-
Total			-	-	14	250	-

II Year II Semester

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R18D6884	Seminar-II	-	-	2	50	-
2	R18D6893	Project Review-II	-	-	8	100	-
3	R18D6894	Project Viva-voce	-	-	8	-	100
Total			-	-	18	150	100

SEMESTER-I

(R18D6801) VLSI TECHNOLOGY AND DESIGN

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology, Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: I_{ds} $-V_{ds}$ relationships, ThresholdVoltage V T , g_m , g_{ds} and ω_o , Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu} /Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:

Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation andtesting.

UNIT –V:

Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005,

PHI.

2. Modern VLSI Design – Wayne Wolf, 3 rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.

2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

(R18D6802) CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex

Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD

Implementation of a Parallel Adder with Accumulation

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and

XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.

4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

(R18D6803) EMBEDDED SYSTEM DESIGN

UNIT –I:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and

Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,

PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions,

Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access

Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

2. Professional Embedded ARM development-James A Langbridge, Wiley/Wrox

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

2. ARM System on Chip Architecture, Steve Furber, 2nd Edition, Pearson

(R18D6807)VLSI SIGNAL PROCESSING

(ELECTIVE-I)

UNIT I:

Introduction To DSP Systems, Pipelining And Parallel Processing Of FIR Filters

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm,

Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II:

Retiming, Algorithmic Strength Reduction

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III:

Fast Convolution, Pipelining and Parallel Processing Of IIR Filters

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV:

Bit-Level Arithmetic Architectures

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V:

Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.

2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

3. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing,

McGraw Hill, 1994

(R18D6808) CMOS ANALOG INTEGRATED CIRCUIT DESIGN

(ELECTIVE-I)

UNIT -I: MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOSDevice Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forthe MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II: Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Currentmirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current andVoltage References, Band gap Reference.

UNIT -III: CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV: CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

UNIT -V: Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University

Press, International Second Edition/Indian Edition, 2010.

2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and

R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.

2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li

(R18D6809) PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

(ELECTIVE-I)

UNIT I:

Embedded 'C' Programming

Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNITII:

Object Oriented Programming

Introduction to procedural, modular, object-oriented and generic programming techniques,

Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT III:

CPP Programming

'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT IV:

Overloading, Inheritance & Templates

Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions

Templates

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw,

Multiple Exceptions.

UNIT V:

Scripting Languages

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script,PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

TEXT BOOKS:

1. Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008

2. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011

3. A. Michael Berman, “Data structures via C++”, Oxford University Press, 2002

4. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999

5. Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey

& Sons, 2005

(R18D6810) CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

(ELECTIVE-II)

UNIT –I:

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,Transistor equivalency, CMOS Inverter logic.

UNIT –II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, ComplexLogic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI andOIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edgetriggered flipflop.

UNIT –IV:

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOStransmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell andrefresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash andNAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,

TMH, 3 rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Press, 2011

2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan,

Borivoje Nikolic, 2 nd Ed., PHI.

(R18D6811)CAD OF DIGITAL SYSTEM

(ELECTIVE-II)

UNIT I:

VLSI Design Methodologies

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II

Design Rules

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III:

Floor Planning

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV:

Simulation

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V:

Modelling And Synthesis

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TEXT BOOKS:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002. 2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002

(R18D6812)SYSTEM DESIGN WITH EMBEDDED LINUX

(ELECTIVE-II)

UNIT I: Embedded OS (Linux) Internals

Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling.

Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

UNIT II: Open source RTOS

Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Metric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS.

UNIT III: Open Source RTOS Issues

POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics, Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.

UNIT IV: VxWorks / Free RTOS

VxWorks/ Free RTOS Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

UNIT V: Case study

Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

TEXT BOOKS:

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan

2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein

3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

REFERENCE BOOKS:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK

3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society

4. Real-time Systems – Jane Liu, PH 2000

5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A

6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J

7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J

8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J

9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H

10. Embedded Software Primer: Simon, David E.

11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw

Hill

(R18DME51) NON-CONVENTIONAL ENERGY SOURCES

(OPEN ELECTIVE-I)

UNIT-I

Introduction: Energy Scenario, Survey of energy resources. Classification and need for conventional energy resources.

Solar Energy: The Sun-sun-Earth relationship, Basic matter to waste heat energy circuit, SolarRadiation, Attention, Radiation measuring instruments.

Solar Energy Applications: Solar water heating. Space heating, Active and passive heating, Energystorage, Selective surface, Solar stills and ponds, solar refrigeration, Photovoltaic generation.

UNIT -II

Geothermal Energy: Structure of earth, Geothermal Regions, Hot springs. Hot Rocks, HotAquifers. Analytical methods to estimate thermal potential. Harnessing techniques, Electricity generating systems.

UNIT-III

Direct Energy Conversion: Nuclear Fusion, Fusion reaction, P-P cycle, Carbon cycle,Deuterium cycle, Condition for controlled fusion, Fuel cells and photovoltaic, Thermionic and Thermoelectric generation and MHD generator.

Hydrogen Gas as Fuel: Production methods, Properties, I.C. Engines applications, Utilization strategy,Performances.

UNIT-IV

Bioenergy: Biomass energy sources. Plant productivity, Biomass wastes, aerobic and anaerobicbioconversion processes, Raw material and properties of bio-gas, Bio-gas plant technology and status, the energetic and economics of biomass systems, Biomass gasification

UNIT-V

Wind Energy: Wind, Beaufort number, Characteristics, Wind energy conversion systems, Types,Betz model. Interference factor. Power coefficient, Torque coefficient and Thrust coefficient, Lift machines and Drag machines. Matching Electricity generation.**Energy from Oceans**: Tidal energy, Tides, Diurnal and semi-diurnal nature, Power from tides, WaveEnergy, Waves, Theoretical energy available. Calculation of period and phase velocity of waves, Wave power systems, submerged devices. Ocean thermal Energy, Principles, Heat exchangers, Pumping requirements, Practical considerations.

TEXTBOOKS:

1.Non-conventional Energy Sources / GD Rai/Khanna publications.
2.Non-Conventional Energy Sources and Utilisation (Energy Engineering)/ R KRajput/ S.Chand.
3.Renewable Energy Sources /Twidell& Weir/Taylor and Francis/ 2nd special Indian edition .

REFERENCE BOOKS:

1.Renewable Energy Resources- Basic Principles and Applications/ G.N.Tiwari and M.K.GhosalNarosa Publications.
2.Renewable Energy Resources/ John Twidell& Tony Weir/Taylor & Francis/2nd edition.

3.Non Conventional Energy / K.Mittal/ Wheeler.

(R18DME52)INDUSTRIAL SAFETY

(OPEN ELECTIVE-I)

UNIT-I:

Industrial safety

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT-II:

Fundamentals of maintenance engineering

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT-III:

Wear and Corrosion and their prevention

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv.Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-IV:

Fault Tracing

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler,vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT-V:

Periodic and preventive maintenance

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance, Repair cycle concept and importance.

TEXTBOOKS:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.

2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.

4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

(R18DME53)OPERATIONS RESEARCH

(OPEN ELECTIVE-I)

UNIT I:

Introduction to OR & Linear Programming

Evolution of OR, definition of OR, scope of OR, application areas of OR, steps (phases) in OR study, characteristics and limitations of OR, models used in OR, linear programming (LP) problem-formulation and solution by graphical method.

Solution Of Linear Programming Problems: The simplex method, canonical and standard form of an LP problem, slack, surplus and artificial variables, big M method and concept of duality, dual simplex method.

UNIT II

Transportation Problem

Formulation of transportation problem, types, initial basic feasible solution using different methods, optimal solution by MODI method, degeneracy in transportation problems, application of transportation problem concept for maximization cases, Assignment Problem-formulation, types, application to maximization cases and travelling salesman problem.

UNIT III:

Integer Programming

Pure and mixed integer programming problems, solution of Integer programming problems-Gomory's all integer cutting plane method and mixed integer method, branch and bound method, Zero-One programming,Pert-CPM Techniques:

Introduction, network construction - rules, Fulkerson's rule for numbering the events, AON and AOA diagrams; Critical path method to find the expected completion time of a project, floats; PERT for finding expected duration of an activity and project, determining the probability of completing a project, predicting the completion time of project; crashing of simple projects.

UNIT IV:

Queuing Theory

Queuing systems and their characteristics, Pure-birth and Pure-death models (only equations), empirical queuing models – M/M/1 and M/M/C models and their steady state performance analysis.

UNIT V:

Game Theory

Formulation of games, types, solution of games with saddle point, graphical method of solving mixed strategy games, dominance rule for solving mixed strategy games.

Sequencing: Basic assumptions, sequencing 'n' jobs on single machine using priority rules, sequencing using Johnson's rule-'n' jobs on two machines, 'n' jobs on three machines, 'n' jobs on 'm' machines. Sequencing two jobs on 'm' machines using graphical method.

TEXTBOOKS:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008

2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.

3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008

4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009

5. Pannerselvam, Operations Research: Prentice Hall of India 2010

6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

(R18DHS51) BUSINESS ANALYTICS

(OPEN ELECTIVE – I)

UNIT I:

Business Analytics

Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics, Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview

UNIT II:

Trendiness and Regression Analysis

Modelling Relationships and Trends in Data, simple Linear Regression, Important Resources, Business Analytics Personnel, Data and models for Business, analytics, problem solving, Visualizing and Exploring Data, Business Analytics, Technology.

UNIT III:

Organization Structures of Business analytics:

Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes, Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics,analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT IV:

Forecasting Techniques

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT V:

Decision Analysis

Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism

TEXT BOOKS:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G.Schniederjans, Christopher M. Starkey, Pearson FT Press.

2. Business Analytics by James Evans, persons Education.

(R18DCS51) Scripting Languages

(OPEN ELECTIVE I)

Objectives: The course demonstrates an in depth understanding of the tools and the scripting languages necessary for design and development of applications dealing with Bio-information/ Bio-data. The instructor is advised to discuss examples in the context of Bio-data/ Bio-information application development.

UNIT I

Introduction to PERL and Scripting Scripts and Programs, Origin of Scripting , Scripting Today, Characteristics of Scripting Languages, Web Scripting, and the universe of Scripting Languages. PERL- Names and Values, Variables, Scalar Expressions, Control Structures, arrays, list, hashes, strings, pattern and regular expressions, subroutines, advance perl - finer points of looping, pack and unpack, filesystem, eval, data structures, packages, modules, objects, interfacing to the operating system, Creating Internet ware applications, Dirty Hands Internet Programming, security Issues.

UNIT II

PHP Basics- Features, Embedding PHP Code in your Web pages, Outputting the data to the browser, Datatypes, Variables, Constants, expressions, string interpolation, control structures, Function, Creating a Function, Function Libraries, Arrays, strings and Regular Expressions.

UNIT III

Advanced PHP Programming Php and Web Forms, Files, PHP Authentication and Methodologies -Hard Coded, File Based, Database Based, IP Based, Login Administration, Uploading Files with PHP, Sending Email using PHP, PHP Encryption Functions, the Mcrypt package, Building Web sites for the World – Translating Websites- Updating Web sites Scripts, Creating the Localization Repository, Translating Files, text, Generate Binary Files, Set the desired language within your scripts, Localizing Dates, Numbers and Times.

UNIT IV

TCL Structure, syntax, Variables and Data in TCL, Control Flow, Data Structures, input/output, procedures, strings, patterns, files, Advance TCL- eval, source, exec and up level commands, Name spaces, trapping errors, event driven programs, making applications internet aware, Nuts

and Bolts Internet Programming, Security Issues, C Interface. Tk- Visual Tool Kits, Fundamental Concepts of Tk, Tk by example, Events and Binding , Perl-Tk.

UNIT V

Python Introduction to Python language, python-syntax, statements, functions, Built-in-functions and Methods, Modules in python, Exception Handling, Integrated Web Applications in Python – Building Small, Efficient Python Web Systems, Web Application Framework.

TEXT BOOKS:

1. The World of Scripting Languages, David Barron, Wiley Publications.

2. Python Web Programming, Steve Holden and David Beazley, New Riders Publications.

3. Beginning PHP and MySQL, 3rd Edition, Jason Gilmore, Apress Publications (Dreamtech)

REFERENCE BOOKS:

1. Open Source Web Development with LAMP using Linux, Apache, MySQL, Perl and PHP, J.Lee and B.Ware (Addison Wesley) Pearson Education.

2. Programming Python, M.Lutz, SPD.

3. PHP 6 Fast and Easy Web Development, Julie Meloni and Matt Telles, Cengage Learning Publications.

4. PHP 5.1,I.Bayross and S.Shah, The X Team, SPD.

5. Core Python Programming, Chun, Pearson Education.

6. Guide to Programming with Python, M.Dawson, Cengage Learning.

7. Perl by Example, E.Quigley, Pearson Education.

8. Programming Perl, Larry Wall, T.Christiansen and J.Orwant, O'Reilly, SPD.

9. Tcl and the Tk Tool kit, Ousterhout, Pearson Education.

10. PHP and MySQL by Example, E.Quigley, Prentice Hall(Pearson).

11. Perl Power, J.P.Flynt, Cengage Learning.

12. PHP Programming solutions, V.Vaswani, TMH.

(R18DAE51) Mathematical Modeling Techniques

(OPEN ELECTIVE I)

UNIT-I: **INTRODUCTION TO MODELING AND SINGULAR PERTURBATION METHODS**

Definition of a model, Procedure of modeling: problem identification, model formulation, reduction, analysis, Computation, model validation, Choosing the model, Singular Perturbations: Elementary boundary layer theory, Matched asymptotic expansions, Inner layers, nonlinear oscillations

UNIT-II: **VARIATIONAL PRINCIPLES AND RANDOM SYSTEMS**

Variational calculus: Euler's equation, Integrals and missing variables, Constraints and Lagrange multipliers, Variational problems: Optics-Fermat's principle, Analytical mechanics: Hamilton's principle, Symmetry: Noether's theorem, Rigid body motion, Random systems: Random variables, Stochastic processes, Monte Carlo method

UNIT-III: **FINITE DIFFERENCES: ORDINARY AND PARTIAL DIFFERENTIAL EQUATIONS**

ODE: Numerical approximations, Runge-Kutta methods, Beyond Runge-Kutta, PDE: Hyperbolic equations-waves, Parabolic equations-diffusion, Elliptic equations-boundary values, **CELLULAR AUTOMATA AND LATTICE GASES:** Lattice gases and fluids, Cellular automata and computing

UNIT- IV: **FUNCTION FITTING AND TRANSFORMS**

Function fitting: Model estimation, Least squares, Linear least squares: Singular value decomposition, Non-linear least squares: Levenberg-Marquardt method, Estimation, Fisher information, and Cramer-Rao inequality, Transforms:Orthogonal transforms, Fourier transforms, Wavelets, Principal components

FUNCTION FITTING ARCHITECTURES: Polynomials: Pade approximants, Splines, Orthogonal functions, Radial basis functions, Over-fitting, Neural networks: Back propagation, Regularization

UNIT-V: **OPTIMIZATION AND SEARCH:** Multidimensional search, Local minima, Simulated annealing, Genetic algorithms **FILTERING AND STATE ESTIMATION:** Matched filters, Wiener filters, Kalman filters, Non-linearity and entrainment, Hidden Markov models

TEXT BOOK:

1. *The Nature of Mathematical Modeling*, Neil Gershenfeld, Cambridge University Press, 2006, ISBN 0-521-57095-6

REFERENCE BOOKS:

1. *Mathematical Models in the Applied Sciences*, A. C. Fowler, Cambridge University Press, 1997, ISBN 0-521-46140-5

2. *A First Course in Mathematical Modeling*, F. R. Giordano, M.D. Weir and W.P. Fox, 2003, Thomson, Brooks/Cole Publishers

3. *Applied Numerical Modeling for Engineers*, Donald De Cogan, Anne De Cogan, Oxford University Press, 1997

(R18DEC51) Embedded Systems Programming

(OPEN ELECTIVE I)

Unit 1 - Embedded OS (Linux) Internals

Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory

Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling.

Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

Unit 2 – Open source RTOS

Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS.

Unit 3 – Open Source RTOS Issues

POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics.

Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.

Unit 4 – VxWorks / Free RTOS

VxWorks/ Free RTOS Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

Unit 5 – Case study

Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

TEXT BOOKS:

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan
2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein
3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

REFERENCES:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
4. Real-time Systems – Jane Liu, PH 2000
5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A
6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J
7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J
8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J
9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H
10. Embedded Software Primer: Simon, David E.
11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

(R18D6881) VLSI LABORATORY

Note:

Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design,Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates

2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, CarryLook Ahead Adder.

3. Design of 2-to-4 decoder

4. Design of 8-to-3 encoder (without and with parity)

5. Design of 8-to-1 multiplexer

6. Design of 4 bit binary to gray converter

7. Design of Multiplexer/ Demultiplexer, comparator

8. Design of Full adder using 3 modeling styles

9. Design of flip flops: SR, D, JK, T

10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequencecounter

11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in

Serial out and Parallel in Parallel Out.

12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).

13. Design of 4- Bit Multiplier, Divider.

14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,

multiplication and Division.

15. Design of Finite State Machine.

16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area,performance and/or power, Layout, Extraction of parasitic and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing Analysis, IR drops analysis and crosstalk analysis of the following:

- Basic logic gates
- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistorBasic logic gates

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

(R18DHS54)VALUE EDUCATION

(Audit Course I)

UNIT I:

Values and self-development

Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non-moral valuation. Standards and principles, Value judgements

UNIT II:

Importance of cultivation of values

Sense of duty, Devotion, Self-reliance, Confidence, Concentration, Truthfulness, Cleanliness,

Honesty, Humanity. Power of faith, National Unity, Patriotism, Love for nature, Discipline

UNIT III:

Personality and Behavior Development

Soul and Scientific attitude, Positive Thinking, Integrity and discipline, Punctuality, Love and Kindness ,Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature

UNIT IV:

Character and Competence

Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence ,Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively

TEXT BOOKS:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

SEMESTER-II

(R18D6804) EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read,write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task asks States and Scheduling, Task Operations, Structure, Synchronization,
Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

(R18D6805) CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

UNIT -II:

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

UNIT -III:

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:

Nyquist Rate A/D Converters:

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

(R18D6806) LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, ShortChannel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, VelocitySaturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.

4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

(R18D6813) ADHOC –WIRELESS NETWORKS
(ELECTIVE -III)

UNIT -I:

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks.

UNIT -II:
MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT -III:
Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT –IV:
Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT –V:
Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:
1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.
REFERENCE BOOKS:
1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh , 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer.

(R18D6814)SOC DESIGN
(ELECTIVE – III)

UNIT I:

ASIC

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT 2:

NISC

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III:

Simulation

Different simulation modes, behavioural, functional, static timing, gate level, switch level,transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV:

Low power SoC design / Digital system

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS),building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V:

Synthesis

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph,Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues,HDL coding techniques for minimization of power consumption, Fault tolerant designs.Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

TEXT BOOKS:

1.Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006
3. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000
4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley,2011

(R18D6815)MEMORY TECHNOLOGIES

(ELECTIVE – III)

UNIT I:

Random Access Memory Technologies

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures,Application Specific SRAMs.

Unit II:

DRAM DESIGN

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

Unit III:

Non-Volatile Memories

Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit IV:

Semiconductor Memory Reliability and Radiation Effects

General Reliability Issues,RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation

Unit V:

Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards,High Density Memory Packaging

TEXT BOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

(R18D6816)PHYSICAL DESIGN AUTOMATION
(ELECTIVE- IV)

UNIT I:
Introduction to VLSI Design Methodologies
Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

UNIT II:
VLSI design automation tools
Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

UNIT III:
General purpose methods for combinational optimization
Partitioning, floor planning and pin assignment, placement, routing. Concepts and Algorithms Modeling: Gate Level Modeling and Simulation, Switch level modeling and simulation, Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis.
Hardware Models: Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

Unit 4:
Simulation
Logic synthesis, verification, high level Synthesis. FPGA technologies: Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models

UNIT V:
MCM technologies
MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing –Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" 3rd edition, Springer International Edition. REFERENCES 1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI" Wiley,1993 2. Wayne Wolf, "Modern VLSI Design: Systems on silicon" Pearson Education Asia, 2nd Edition.

(R18D6817)COMMUNICATION BUSES AND INTERFACES
(ELECTIVE- IV)

Unit 1:
Serial Buses: Physical interface, Data and Control signals, features

Unit 2:
Limitations and applications of RS232, RS485, I2C, SPI

Unit 3:
CAN Architecture, Data transmission, Layers, Frame formats, applications

Unit 4:
PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit 5:
USB - Transfer types, enumeration, Descriptor types and contents, Device driver
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

TEXT BOOKS:
1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition
2.Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x

(R18D6818) MULTIMEDIA AND SIGNAL CODING
(ELECTIVE-IV)

UNIT-I:

Introduction to Multimedia

Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT-II:

Video Concepts: Types of Video Signals, Analog Video, Digital Video.

Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT-III:

Compression Algorithms

Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

Image Compression Standards: JPEG and JPEG2000.

UNIT-IV:

Video Compression Techniques

Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and InterFrame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT-V:

Audio, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009.

REFERENCE BOOKS:

1. Multimedia Communication Systems – Techniques, Stds & Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A. Milovanovic, 1st Edition, 2002.

2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

(R18DME54) Composite Materials (OPEN ELECTIVE II)

UNIT–I: Introduction: Definition – Classification and characteristics of Composite materials, Advantages and application of composites. Functional requirements of reinforcement and matrix, Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II: **Reinforcements:** Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures, Isostrain and Isostress conditions.

UNIT – III: Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV: Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection, Moulding, Properties and applications.

UNIT – V: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

References:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W.Tasi.

(R18DME55) Waste to Energy (OPEN ELECTIVE II)

UNIT-I: Introduction to Energy from Waste

Classification of waste as fuel – Agro based, Forest

residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT-II: Biomass Pyrolysis

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods -Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT-III: Biomass Gasification

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers –Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT-IV: Biomass Combustion:

Biomass stoves – Improved chullahs, types, some exotic designs,Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design,construction and operation - Operation of all the above biomass combustors.

UNIT-V: Biogas

Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their Classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion -Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production -Urban waste to energy conversion - Biomass energy programme in India.

References:

1. Hand Book of Composite Materials-ed-Lubin.

2. Composite Materials – K.K.Chawla.

3. Composite Materials Science and Applications – Deborah D.L. Chung.

4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W.Tasi.

(R18DME56) Industrial Management (OPEN ELECTIVE II)

Objective:

To introduce the fundamental concepts and techniques in computer and network security, giving students an overview of information security and auditing, and to expose students to the latest trend of computer attack and defense. Other advanced topics on information security such as mobile computing security, security and privacy of cloud computing, as well as secure information system development will also be discussed.

UNIT IA model for Internetwork security, Conventional Encryption Principles & Algorithms (DES, AES, RC4, Blowfish), Block Cipher Modes of Operation, Location of Encryption Devices, Key Distribution.

Public key cryptography principles, public key cryptography algorithms (RSA, Diffie-Hellman, ECC), public Key Distribution.

UNIT II Approaches of Message Authentication, Secure Hash Functions (SHA-512, MD5) and HMAC, Digital Signatures, Kerberos, X.509 Directory Authentication Service, Email Security: Pretty Good Privacy (PGP)

IP Security: Overview, IP Security Architecture, Authentication Header, Encapsulating Security Payload, Combining Security Associations and Key Management.

UNIT III Web Security: Requirements, Secure Socket Layer (SSL) and Transport Layer Security (TLS), Secure Electronic Transaction (SET). Firewalls: Firewall Design principles, Trusted Systems, Intrusion Detection Systems

UNIT IV Auditing For Security: Introduction, Basic Terms Related to Audits, Security audits, The Need for Security Audits in Organization, Organizational Roles and Responsibilities for Security Audit, Auditors Responsibility In Security Audits, Types Of Security Audits.

UNIT V Auditing For Security: Approaches to Audits, Technology Based Audits Vulnerability Scanning And Penetration Testing, Resistance to Security Audits, Phase in security audit, Security audit Engagement Costs and other aspects, Budgeting for security audits, Selecting external Security Consultants, Key Success factors for security audits.

TEXT BOOKS:

1. Cryptography and Network Security by William Stallings, Fourth Edition, Pearson Education 2007.

2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education, 2008.

3. Cryptography & Network Security by Behrouz A. Forouzan, TMH 2007.

4. Information Systems Security by Nina Godbole, WILEY 2008.

REFERENCE BOOKS:

1. Information Security by Mark Stamp, Wiley – INDIA, 2006.

2. Fundamentals of Computer Security, Springer.

3. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH

4. Computer Security Basics by Rick Lehtinen, Deborah Russell & G.T.Gangemi Sr., SPD O'REILLY 2006.

5. Modern Cryptography by Wenbo Mao, Pearson Education 2007.

6. Principles of Information Security, Whitman, Thomson.

(R18DHS52)COST MANAGEMENT OF ENGINEERING PROJECTS
(OPEN ELECTIVE –II)

UNIT I:

Introduction and Overview of the Strategic Cost Management Process

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunitycost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II:

Project:

Meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member,Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control,Bar charts and Network diagram.

UNIT III:

Project commissioning

mechanical and process Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis.

UNIT IV:

Pricing strategies

Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.

UNIT V:

Budgetary Control

Flexible Budgets, Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

TEXT BOOKS:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting

(R18DCS52) Information Security (OPEN ELECTIVE II)

Objective:

To introduce the fundamental concepts and techniques in computer and network security, giving students an overview of information security and auditing, and to expose students to the latest trend of computer attack and defense. Other advanced topics on information security such as mobile computing security, security and privacy of cloud computing, as well as secure information system development will also be discussed.

UNIT I

A model for Internetwork security, Conventional Encryption Principles & Algorithms (DES, AES, RC4, Blowfish), Block Cipher Modes of Operation, Location of Encryption Devices, Key Distribution.

Public key cryptography principles, public key cryptography algorithms (RSA, Diffie-Hellman, ECC), public Key Distribution.

UNIT II

Approaches of Message Authentication, Secure Hash Functions (SHA-512, MD5) and HMAC, Digital Signatures, Kerberos, X.509 Directory Authentication Service, Email Security: Pretty Good Privacy (PGP)

IP Security: Overview, IP Security Architecture, Authentication Header, Encapsulating Security Payload, Combining Security Associations and Key Management.

UNIT III

Web Security: Requirements, Secure Socket Layer (SSL) and Transport Layer Security (TLS), Secure Electronic Transaction (SET). Firewalls: Firewall Design principles, Trusted Systems, Intrusion Detection Systems

UNIT IV

Auditing For Security: Introduction, Basic Terms Related to Audits, Security audits, The Need for Security Audits in Organization, Organizational Roles and Responsibilities for Security Audit, Auditors Responsibility In Security Audits, Types Of Security Audits.

UNIT V

Auditing For Security: Approaches to Audits, Technology Based Audits Vulnerability Scanning And Penetration Testing, Resistance to Security Audits, Phase in security audit, Security audit Engagement Costs and other aspects, Budgeting for security audits, Selecting external Security Consultants, Key Success factors for security audits.

TEXT BOOKS:

1. Cryptography and Network Security by William Stallings, Fourth Edition, Pearson Education 2007.

2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education, 2008.

3. Cryptography & Network Security by Behrouz A. Forouzan, TMH 2007.

4. Information Systems Security by Nina Godbole, WILEY 2008.

REFERENCE BOOKS:

1. Information Security by Mark Stamp, Wiley – INDIA, 2006.

2. Fundamentals of Computer Security, Springer.

3. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH

4. Computer Security Basics by Rick Lehtinen, Deborah Russell & G.T.Gangemi Sr., SPD O'REILLY 2006.

5. Modern Cryptography by Wenbo Mao, Pearson Education 2007.

6. Principles of Information Security, Whitman, Thomson.

(R18DAE52) UNMANNED AERIAL VEHICLES (OPEN ELECTIVE II)

UNIT-I: INTRODUCTION TO UNMANNED AIRCRAFT SYSTEMS

Applications of UAS, categories of UAV systems, roles of unmanned aircraft, composition of UAV system.

UNIT-II: DESIGN OF UAV SYSTEMS-I

Introduction to design and selection of the systems-conceptual phase, preliminary design, detailed design; Aerodynamics and airframe configurations-Lift-induced Drag, Parasitic Drag, Rotary-wing Aerodynamics, Response to Air Turbulence, Airframe Configurations; Medium-range, Tactical Aircraft, Characteristics of Aircraft Types-Long-endurance, Long-range Role Aircraft, Medium-range, Tactical Aircraft, Close-range/Battlefield Aircraft, MUAV Types, MAV and NAV Types, UCAV, Novel Hybrid Aircraft Configurations, Aspects of Airframe Design: Scale Effects, Packaging Density, Aerodynamics, Structures and Mechanisms, Selection of power-plants, Modular Construction, Ancillary Equipment, Design for Stealth: Acoustic Signature, Visual Signature, Thermal Signature, Radio/Radar Signature, Payload Types: Non-dispensable and dispensable payloads.

UNIT-III: DESIGN OF UAV SYSTEMS-II

Communications-Communication Media, Radio Communication, Mid-air Collision (MAC) Avoidance, Communications Data Rate and Bandwidth Usage, Antenna Type; Control and Stability: HTOL Aircraft, Convertible Rotor Aircraft, Payload Control, Sensors, Autonomy; Navigation: NAVSTAR Global Positioning System (GPS), TACAN, LORAN C, Inertial Navigation, Radio Tracking, Way-point Navigation; Launch and Recovery.

Design for Reliability: Determination of the Required Level of Reliability, Achieving Reliability, Reliability Data Presentation, Multiplexed Systems, Reliability by Design, Design for Ease of Maintenance; Design for Manufacture and Development

UNIT-IV: THE DEVELOPMENT OF UAV SYSTEMS

System Development and Certification-System Development, Certification, Establishing Reliability; System Ground Testing: UAV Component Testing, UAV Sub- assembly and Sub-system Testing, Testing Complete UAV, Control Station Testing , Catapult Launch System Tests, Documentation; System In- flight Testing: Test Sites, Preparation for In-flight Testing, In- flight Testing, System certification.

UNIT-V: DEPLOYMENT AND FUTURE OF UAV SYSTEMS

Operational trials and full certification; UAV System Deployment- Network-centric Operations (NCO), Teaming with Manned and Other Unmanned System; Naval, arm and air force roles, civilian, paramilitary and commercial roles.

Text Books:

1. Reg Austin, Wiley, “Unmanned Aircraft Systems, UAVS Design and Deployment”, 2nd Edition, 2010.

Reference Books:

1. Richard K. Barnhart, Stephen B. Hottman, Douglas M. Marshall, Eric Shappee, (eds.), “Introduction to Unmanned Aircraft Systems”, CRC Press, 2012.

2. Valavanis, Kimon P., Vachtsevanos, George J. “Handbook of Unmanned Aerial Vehicles” AIAA series, 3rd Edition, 2004.

(R18DHS53) RESEARCH METHODOLOGY
(OPEN ELECTIVE – II)

UNIT - I

Introduction: Research objective and motivation, Types of research, Research approaches, Significance, Research method vs. methodology, Research process.

UNIT - II

Formulating a research problem: Literature review, Formulation of objectives, Establishing Operational definitions, Identifying variables, constructing hypotheses.

UNIT - III

Research design and Data Collection: Need and Characteristics, Types of research design, Principles of Experimental research design, Method of data collection, Ethical issues in collecting data.

UNIT - IV

Sampling and Analysis of data: Need of Sampling, Sampling distributions, Central limit theorem, Estimation: mean and variance, Selection of sample size Statistics in research, Measures of Central tendency, Dispersion, asymmetry and relationships, Correlation and Regression analysis, Displaying data

UNIT - V

Hypothesis Testing: Procedure, Hypothesis testing for difference in mean, variance limitations, Chi-square test, Analysis of variance (ANOVA), Basic principles and techniques of writing a Research Proposal

Text Books:

1. R. C. Kothari, Research Methodology: Methods and Techniques, 2nd edition, New Age International Publisher, 2009

2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners, 2nd Edition, SAGE, 2005

References:

1. Trochim, William M. The Research Methods Knowledge Base, 2nd Edition. Internet WWW page, at URL: <http://www.socialresearchmethods.net/kb/>

2. (Electronic Version): StatSoft, Inc. (2012). Electronic Statistics Textbook. Tulsa, OK: StatSoft. WEB: http://www.statsoft.com/textbook/.(Printed Version): Hill, T. & Lewicki, P. (2007). STATISTICS: Methods and Applications. StatSoft, Tulsa, OK.

(R18D6882) EMBEDDED SYSTEMS LABORATORY

Note:
The following programs are to be implemented on ARM based Processors/Equivalent.
Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

Part -I: The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division
b. Operating Modes, System Calls and Interrupts
c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

Part -II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

(R18DHS55)ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE II)

UNIT I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and vagueness

UNIT II:

Clarifying Who Did What, Highlighting Your Findings, Hedging, and Critics in paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

UNIT V:

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions: useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

COURSE COVERAGE SUMMARY & QUESTION BANK-SEMESTER-I

VLSI TECHNOLOGY AND DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Essentials of VLSI Circuits and Systems	1,2	UNIT-I:Review of Microelectronics and Introduction to MOS Technologies	K. Eshraghian Eshraghian. D, A. Pucknell	PHI	2005
2	Modern VLSI Design	2,3	UNIT –II: Layout Design and Tools	Wayne Wolf	Pearson Education	3 rd Ed
3	Modern VLSI Design	4	UNIT –II: Combinational Logic Networks	Wayne Wolf	Pearson Education	3 rd Ed
4	Modern VLSI Design	5	UNIT –IV: Sequential Systems	Wayne Wolf	Pearson Education	3 rd Ed
5	Modern VLSI Design	7,8	UNIT –V: Floor Planning	Wayne Wolf	Pearson Education	3 rd Ed

R17

Code No: R17D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

VLSI Technology & Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*****

SECTION - I

1.	a)	With neat sketches, explain the different steps in the NMOS fabrication process	7M
	b)	Draw the circuit diagram of a nMOS inverter and explain its operation. Also plot its transfer characteristics	7M

OR

2.	a)	Compare CMOS and Bipolar technologies	7M
	b)	Describe the latch-up problem in CMOS circuits and its prevention	7M

SECTION – II

3.	a)	Draw the physical structure of a MOS transistor and describe the layout rules of nMOS and pMOS transistors	7M
	b)	Draw the circuit diagram, stick diagram and complete mask layout of Y′ = A(B+C) (with a clear indication of all the layers)	7M

OR

4.	a)	Sketch the stick diagram and complete mask layout of a CMOS inverter and clearly indicate the different layers	7M
	b)	Compare alternate gates like pseudo NMOS and DVSL with static complementary CMOS gates with neat circuit diagrams	7M

SECTION – III

5.	a)	Explain the routing issues in standard cell design methodology	7M
	b)	Describe the various techniques used for computing and minimizing power dissipation in combination logic networks	7M

OR

6.		Discuss the process and need of layout, simulation in combinational logic network	14M

SECTION – IV

7.		Explain the design validation and testing for a sequential logic systems	14M

OR

8.	a)	Define the setup-time and hold-time of a flip flop and describe the setup-time constraint and hold-time constraint in a timing path	7M
	b)	Describe some techniques for optimizing power dissipation in sequential circuits	7M

SECTION – V

9.	a)	Distinguish between floorplanning and leaf-cell design? Give an example of a floorplan for a large chip	7M
	b)	Draw the structure of a typical IC package and indicate the different parts clearly. Also provide a list of commonly used IC packages	7M

OR

10.	a)	Explain the various wiring layers available for interconnect and discuss the design issues in power distribution	7M
	b)	Define the terms (i) pad (ii) pad frame and (iii) electrostatic discharge (with diagrams)	7M

****

Code No: **R18D6801**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

VLSI Technology & Design

(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION - I

1. a) Define Moore's Law and Compare the various device technologies used in Integrated circuits [7M]
   b) Derive the Id vs Vds relationship of a MOS transistor [7M]

OR

2. With neat diagrams, explain the operation of a MOS transistor. Distinguish between enhancement mode and depletion mode transistor [14M]

SECTION – II

3. a) Explain the wires and vias in integrated circuits along with a description of their capacitor parasitics [7M]
   b) Draw the circuit diagram, stick diagram and complete mask layout of 2-input NAND gate (with a clear indication of all the layers) [7M]

OR

4. a) What is meant by a stick diagram and layout diagram and give the stick encodings of layout encodings for MOS layers [7M]
   b) Explain the various techniques for minimizing the power dissipation of logic gates [7M]

SECTION – III

5. a) Describe the standard cell layout methodology for preparing large layouts [7M]
   b) Explain the different techniques used for computing and minimizing interconnect delays [7M]

OR

6. a) What is the need for simulation? Explain the various types of simulation used in integrated circuit design [7M]
   b) Describe the use of MOS transistors as switches in building logic gates [7M]

SECTION – IV

7. a) Distinguish between latches and flip-flops. Define setup-time, hold time and propagation delay of flip-flops [7M]
   b) What is the limitation of a single phase clock? Explain the method to overcome it [7M]

OR

8.	a)	Explain the sequential system design with a circuit example	[7M]
	b)	Explain the testing of sequential system with an example	[7M]

SECTION – V

9.	a)	What is the need for floor planning? Discuss the steps in floor plan design.	[14M]

OR

10.	a)	Explain the design issues in block placement and channel definition with neat examples	[7M]
	b)	Describe the different rules of thumb in floor plan design	[7M]

****

Code No: R17D6801 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018

VLSI Technology& Design

(VLSI& ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION - I

1.(a) What are the electrical properties of MOS and CMOS. (7m)

(b) Compare CMOS and BiCMOS technologies. (7m)

or

2 (a) Draw the diagram of CMOS & BiCMOS inverters and explain about them. (7m)

(b) List out the limitations of MOS and BiCMOS technologies. (7m)

SECTION - II

3.(a) What is the need of Layout design, Explain about the latest layout design and give its significance. (7m)

(b) List out various Scalable design rules and explain about them. (7m)

or

4 (a) Compare resistive and inductive interconnect delays. (7m)

(b) Explain in detail about Static complementary gates with example. (7m)

SECTION - III

5 Explain in detail about the following with respect to Combinational logic networks.

i) Layouts (7m)

ii) Gate testing (7m)

Or

6 Explain in detail about Interconnect design with example with respect to switch logic networks. (14m)

SECTION – IV

7 What is the need of Design validations and testing with respect to sequential systems and explain about them. (14m)

Or

8 What do you understand by the term Clocking disciplines and explain about them in detail. (14m)

SECTION – V

9 Discuss in detail about Global interconnect with regards to Floor Planning. (14m)

Or

10 What is the need of Floor planning methods and explain in detail any two methods (14m)

R15

Code No: R15D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018

VLSI Technology & Design

(VLSI& ES)

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

Section-I

1.a. With a neat diagram ,Explain CMOS Inverter voltage transfer characteristics with a neat diagram? 8M

b. Compare CMOS and Bipolar technologies. 7M

Or

2.aDerive the relevant expressions I_{ds} versus V_{ds} in the non saturated and saturated regions.8M

b.Briefly explain about V_t, g_m,g_{ds}, w_o of MOS transistor.7M

Section-II

3.a What are the varieties of design layout of wiring trees in the wires and delay? 8M

b. What are design rules? Why is metal-metal spacing larger then poly-poly spacing preferred? 7M

Or

4.a. What are lambda based design rules? Give them for each layer. 8M

b. Draw the stick diagram of 2-input Ex-or gate. 7M

Section-III

5.a. How the standard cell layout design of a combinational logic network is implemented? Explain. 8M

b. Mention the various approaches of routing techniques to equalize channel utilization. 7M

Or

6.a. What are the problems presented by power distribution? How they are solved? 8M

b. How fan-out and path delay influences delay in combinational networks.Explain. 7M

Section-IV

7. Explain about clocking diciplines 15M

Or

8. Explain the methods for testing faulty gate in a combinational network. 15M

Section-V

9.a. Briefly Explain about floor planning methods. 8M

b.What are various interconnect models and the factors effecting inter connect performance. 7M

Or

10.a.Name the purposes and basic ideas for floor planning? 8M

b. Discuss the design of floor plan and its considerations? 7M

****

R15

Code No: **R15D6801**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

VLSI Technology & Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

Section-I

Q. No. 1 a) Derive the $I_{ds} - V_{ds}$ relationships and figure of merit of a NMOS transistor (10M)

b) Discuss about the Latch-up in CMOS circuits with suitable diagrams. (5M)

OR

Q. No. 2 a) Explain the CMOS fabrication using N-well process with neat diagrams (8M)

b) Compute the Z_{pu}/Z_{pd} when the inverter is driven by one or more pass transistors. (7M)

Section-II

Q. No. 3 a) Discuss about the Scalable design rules in detail with relevant diagrams (10M)

b) Draw the structure of AND-NAND logic using DCVSL (5M)

OR

Q. No. 4 a) Draw the layout diagram of a static complementary gate that computes [a (b+c)]' (10M)

b) Discuss about any one method used in the design of low power gates (5M)

Section-III

Q. No. 5 a) Categorize the types of Simulators and explain the switch level simulation. (5M)

b) How could you determine the fault testing for combinational networks? (5M)

c) What changes would you make to optimize the power consumption ? (5M)

OR

Q. No. 6 a) Can you elaborate how to design logic networks using realistic interconnect models? (8M)

b) Briefly discuss about the Left-edge channel routing and channel density in standard cell layout. (7M)

Section-IV

Q. No. 7 a) Discuss in detail about Clocking disciplines to construct a sequential system (12M)

b) Draw the structure of an LSSD latch. (3M)

OR

Q. No. 8 Explain briefly about design validation and testing. (15M)

Section-V

Q. No. 9 briefly discuss about the Floor Planning Methods. (15M)

OR

Q. No. 10 a) Explain the Floor Plan Design (7M)

b) Briefly discuss about the I/O architecture and Pad design (8M)

Code No: R17D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

VLSI Technology & Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

SECTION - I

1.(a) Differentiate between CMOS and BICMOS technologies. (7M)

(b) Explain in detail about Latch –up in CMOS circuits. (7M)

(OR)

2 (a) Discuss in detail about MOS Transistor circuit model. (7M)

(b) Draw and explain the operation of CMOS inverter and its characterstics. (7M)

SECTION - II

3.(a) List out various Layout design tools and explain about them. (7M)

(b) Explain with example in detail, about Wires and Vias. (7M)

(OR)

4 (a) What are Static complementary gates .Explain about them in detail. (7M)

(b) Compare the Scalable design rules and Layout design . (7M)

SECTION – III

5 Define the term Power Optimization and explain about the term related to combinational logic networks .(14M)

(OR)

6 With respect to combinational logic circuits, explain the following terms

(i) Network delay (7M)

(ii) Network testing (7M)

SECTION – IV

7 Explain the concept of Power Optimization for Sequential systems with an example. (14M)

(OR)

8 List out and explain about the Memory cells and Array with respect to the sequential circuits (14M)

SECTION – V

9 What is the need of floor planning methods and explain in details any two methods. (14M)

(OR)

10 What are Off–chip connections? List out the advantages and limitations. (14M)

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS
1	Digital Systems Design	2,3	Unit I- Introduction to Programmable Logic Devices	Charles H. Roth Jr, Lizy Kurian John	Cengage Learning
2	Field Programmable Gate Array Technology	2,3	UNIT-II: Field Programmable Gate Arrays	Stephen M. Trimberger,	Springer International Edition
3	Field Programmable Gate Array Technology	4	UNIT -III: SRAM Programmable FPGAs	Stephen M. Trimberger,	Springer International Edition
4	Field Programmable Gate Array Technology	5	UNIT -IV: Anti-Fuse Programmed FPGAs	Stephen M. Trimberger,	Springer International Edition
5	Field Programmable Gate Array Technology	7,8	UNIT -V: Design Applications	Stephen M. Trimberger,	Springer International Edition

Code No: **R17D6802**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

CPLD & FPGA Architectural Applications
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*****

SECTION-I

1 Implement a sequential machine in ROM whose state table is given below **[8M]**

	NS		Z	
PS	$X=0$	$X=1$	$X=0$	$X=1$
S_0	S_1	S_2	1	0
S_1	S_3	S_4	1	0
S_2	S_4	S_4	0	1
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_0	—	1	—

b) Distinguish among the PROM, PLA, and PAL? **[6M]**

2 a) Implement a Parallel Adder with Accumulator using CPLD **[7M]**
b) Explain the architectur of Xilinx cool runner XCR3064XL CPLD? **[7M]**

SECTION-II

3 a) How could you classify the FPGA architectures and illustrate them with neat figures **[8M]**
b) How would you implement the function $F_1 = A^1 B^1 C + A^1 BC^1 + AB$ using an FPGA with programmable logic blocks. Explain the implementation procedure. **[6M]**

OR

4 a) Discuss the dedicated specialized components in FPGAs with example architecture in detail. **[10M]**

b) Compare the FPGA programming technologies **[4M]**

SECTION-III

5 a) Discuss the SRAM-programmable FPGA memory cell configurations **[8M]**

b) Draw the Island-Style SRAM-Programmable FPGA Architecture and identify the building blocks. **[6M]**

OR

6 a) Can you elaborate the architecture of XC4000. **[10M]**

b) Briefly discuss the advantages and Disadvantages of SRAM Programming **[4M]**

SECTION-IV

7 a) Which programming technology is used in Actel architectures? Elaborate the reasons including the programming element construction **[10M]**

b) Discuss the Programming Sneak Path in Act3. **[4M]**

OR

8 Explain the speed performance of Actel ACT1, ACT2 and ACT3 with architecture.

[14M]

SECTION-V

9 a) Describe the block diagram of a fast Video Controller. **[7M]**

b) Design a fast DMA controller. **[7M]**

OR

10 a) Discuss the functionality of high-precision robot manipulator **[7M]**

b) Design a fast binary Counter using CLB **[7M]**

****

R18

Code No: R18D6802

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

CPLD & FPGA Architectures Applications
(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1 a) Design a PLA that realizes the following functions: **[7M]**
$F0 = \sum m\ (0, 1, 4, 6)$, $F1 = \sum m\ (2, 3, 4, 6, 7)$, $F2 = \sum m\ (0, 1, 2, 6)$, $F3 = \sum m\ (2, 3, 5, 6, 7)$.

b) Illustrate the classification of popular programmable logic devices with relevant diagram. **[7M]**

OR

2 Briefly explain the concept of CPLD and Discuss in detail the architecture of Xilinx Cool Runner XCR3064XL CPLD, its macro cell with neat diagram. **[14M]**

SECTION-II

3 a) Discuss in detail about a configurable input/output block (I/OB) in FPGAs with neat diagram? **[8M]**
b) Briefly explain any two programming technologies in FPGA

[6M]

OR

4 Discuss the Interconnects, routing in symmetric array FPGAs and the reason for clock skew **[14M]**

SECTION-III

5 How would you address the design tradeoffs in commercial FPGA architectures **[14M]**

OR

6 Identify the additional features of XC4000. Discuss the XC4000 architecture wiring architecture interconnects in detail. **[14M]**

SECTION-IV

7 a) Elaborate the principles of programmable Anti fuse routing **[8M]**

b) Discuss the Act1 logic module with neat diagram **[6M]**

OR

8 Identify the key features in Act3 compared to Act 2 architecture. Discuss the Act3 S-module; I/O module and anti fuse programming in detail with relevant diagrams. **[14M]**

SECTION-V

9 a) Describe a position tracker for a Robot Manipulators. **[7M]**

b) Design a Act2 Six-Bit Loadable Counter. **[7M]**

OR

10 a) Describe the block diagram of high-speed DMA Controller and its layout. **[8M]**

b) Design a Fast video Controllers. **[6M]**

****

R17

Code No: **R17D6802**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018

CPLD& FPGA Architectures Applications

(VLSI& ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

****

Section-I

Q. No. 1 a) Design a XNOR gate with PLA and PAL (7M)

b) Design a XOR gate with PROM and ROM (7M)

OR

Q. No. 2 a) Design a Boolean expression f=AB+BC+CA with PROM (7M)

b) Design a Boolean expression f=ABC+BCD+CA with PLA (7M)

Section-II

Q. No. 3 a) Explain FPGA state machine terms: i) State transition table, ii) State table. (7M)

b) What are the basic concepts and properties of Petrinet and explain it. (7M)

OR

Q. No. 4 a) Explain the design flow of CPLD and FPGA. (7M)

b) Mention various digital front end digital design tools for FPGA & ASICs. (7M)

Section-III

Q. No. 5 a) Draw and explain the architecture of Cypress Flash 370 CPLD. (7M)

b) Mention the features of a Lattice isp & PLSI's 3000 series. (7M)

OR

Q. No.6 a) Draw the architecture of Xilinx XC 2000 CLB and explain it. (7M)

b) Explain the routing architecture of Xilinx XC 2000. (7M)

Section-IV

Q. No. 7 a) Explain different programming technologies used in CPLD and FPGA. (7M)

b) What are the features and applications of FPGA? (7M)

OR

Q. No. 8 a) what are difference between the ACT1 & ACT2 (7M)

b) What are differences between the ACT2 & ACT3 (7M)

Section-V

Q. No. 9 Implement the Excess 3 to BCD code converter Finite State Machine with PLA. (7M)

OR

Q. No. 10 Implement the BCD to Excess 3 code converter Finite State Machine with PROM. (7M)

Code No: **R17D6802**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

CPLD & FPGA Architectures Applications

(VLSI&ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

Section-I

Q. No. 1 a) Design a full subtractor circuit using ROM (7M)

b) Design a full adder circuit using PAL (7M)

OR

Q. No. 2 a) Draw and explain the architecture of ROM and EPROM. (7M)

b) Design a Half adder & Subtractor circuit using PAL (7M)

Section-II

Q. No. 3 a) Explain the applications of FPGAs (7M)

b) Explain the Programmable I/O blocks in FPGAs (7M)

OR

Q. No. 4 a) Explain generalized FPGA architecture with a neat block diagram. (7M)

b) Explain the Programmable Interconnects in FPGAs (7M)

Section-III

Q. No. 5 a) Draw the architecture of Xilinx XC 4000 CLB and explain it. (7M)

b) Explain the routing architecture of Xilinx XC 4000 (7M)

OR

Q. No.6 a) Draw the architecture of Xilinx XC 3000 CLB and explain it (7M)

b) Explain the routing architecture of Xilinx XC 2000 (7M)

Section-IV

Q. No. 7 a) Explain the Programming Technology of ACT1 (7M)

b) Explain different Programming Technologies used in CPLD &FPGA (7M)

OR

Q. No. 8 a) Explain the Device Architecture, The Actel ACT2 (7M)

b) Explain the Programming Technology of ACT3 (7M)

Section-V

Q. No. 9 a) Explain and draw the diagram with FPGA a Position Tracker for a Robot Manipulator. (7M)

b) Explain about a fast DMA controller (7M)

OR

Q. No. 10 Implement the Excess 3 to BCD code converter Finite State Machine with PLA. (14M)

EMBEDDED SYSTEM DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	CHAPTERS IN TEXT BOOK	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	ARM Systems Developer's Guides- Designing & Optimizing System Software	1,2	UNIT –I: ARM Architecture	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
2	ARM Systems Developer's Guides	3	UNIT –II: ARM Programming Model – I	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
3	ARM Systems Developer's Guides	4	UNIT –III: ARM Programming Model – II	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008
4	ARM Systems Developer's Guides	5,6	UNIT –IV: ARM Programming	Andrew N. Sloss, Dominic Symes, Chris	Elsevier	2008

				Wright		
5	ARM Systems Developer's Guides	12	UNIT –V: Memory Management	Andrew N. Sloss, Dominic Symes, Chris Wright	Elsevier	2008

Code No: **R15D9303**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

Embedded System Design
(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

*****

SECTION-I

1 a) With a neat sketch discuss ARM programming model. **[15M]**
b) What do you mean by pipelining? Briefly discuss about five stage pipeline in ARM.

OR

2 Explain how to measure the processor performance of an embedded hardware in detail and explain the major application areas of embedded system. **[15M]**

SECTION-II

3 a)Explain Load, store instructions with examples. **[15M]**
b) What is the primary difference between a load/store architecture and a register/memory architecture

OR

4 a) What are the unique features of the ARM instruction set? Explain **[7M]**
b) Briefly explain the ARM data processing instructions in detail with suitable example. **[8M]**

SECTION-III

5 Explain processor modes of ARM7 , also specify different branch instruction used to exchange branch from ARM mode to THUMB mode. **[15M]**

OR

6 Draw the format of ARM data processing instructions **[15M]**

Explain the various data operations in ARM.

SECTION-IV

7 a) Explain the different features of FPA10. **[15M]**
b) Discuss the coprocessor Register transfer instructions? Why the instruction cannot used for Register transfer of CP15 coprocessor.

OR

8 Briefly explain the functions, pointers and structures using in ARM C programming **[15M]**

SECTION-V

9 a) With a neat diagram discuss set associate cache and fully associative cache. **[15M]**
b) Elaborate advantages of having embedded memory on chip? How it is useful in increasing the efficiency of the system.

OR

10 What are the different types of memories used in embedded system design? Explain each with examples. **[15M]**

****

R17

Code No: R17D9303

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

Embedded System Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*****

SECTION-I

1	a.	Describe the complete ARM register set ?	**[7M]**
	b.	Describe the conditional flags of ARM processor?	**[7M]**

OR

2	a.	Describe the ARM nomenclature and architecture evaluation ?	**[7M]**
	b.	Describe the pipelining execution process in ARM ?	**[7M]**

SECTION-II

3		Describe various addressing modes in ARM ?	**[14M]**

OR

4		Describe load-store instruction in detail ?	**[14M]**

SECTION-III

5		Explain various thumb data processing instruction ?	**[14M]**
		OR	
6		Explain with example single-register and multiple-register load-store instruction?	**[14M]**

SECTION-IV

7	a.	Explain pointer aliasing with an example?	**[7M]**
	b.	Explain with example conditional execution ?	**[7M]**
		OR	
8	a.	ARM9TDMI processor performs various operations in parallel explain them in detail?	**[10M]**
	b.	What is pipeline interlock explain with example **?**	**[4M]**

SECTION-V

9	a.	How is memory organised in MMU?	**[7M]**
	b.	Explain access permission in memory management	**[7M]**
		OR	
10	a.	Explain flush and clean operation in cache?	**[7M]**
	b.	What are the main software configuration and control components in MMU? Explain in detail any two?	**[7M]**

****

R15

Code No: R15D9303

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

Embedded System Design
(SSP,VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

***

SECTION-I

1 a) Compare various versions of ARM with respect to features, power dissipation and advantages. **[7M]**

b) Distinct between traditional organization and modern organization. **[8M]**

OR

2 What is the difference between microprocessor and micro controller? Explain the role of controllers and microprocessors in embedded system design. **[7M]** **[8M]**

SECTION-II

3 Explain about PSR instructions by giving examples **[15M]**

OR

4 Explain addressing modes of ARM7TDMI. **[15M]**

SECTION-III

5	a) ARM processor is in fact two processors in on chip ARM and THUMB. Explain why two processors are built in one system?	**[5M]**
	b) The ARM processor uses 32 bit code making it possible to provide multiple operations in a single instruction. Explain a few typical instructions.	**[5M]**
	c) The interrupt service is quite powerful in ARM. Explain the need for a fast interrupt service and a normal interrupt service with their own stack operations.	**[5M]**

OR

6	Explain data processing arithmetic instructions with example. (ADD, ADC, ADDS, SUB, SBC, SUBS, MUL, MAL, etc)	**[15M]**

SECTION-IV

7	Explain AREA, CODE, END, LTORG directive of ARM assembly program	**[15M]**

OR

8	Explain data structures queue, circular queue, Linked list, Array.	**[15M]**

SECTION-V

9	Write short notes on the following: a) situation switching. b) Data kinds in ARM. c) Condition execution.	**[5M]** **[5M]** **[5M]**

OR

10	a) Discuss the ARM MMU architecture. b) How the synchronization is occurred ranging from the different processes in ARM. Discuss.	**[7M]** **[8M]**

****

R18

Code No: R18D6803

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

Embedded System Design
(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1 a. How ARM instruction set differs from pure RISC for embedded systems? **[7M]**
b. Explain the Registers and control program status register in ARM ? **[7M]**

OR

2 a. Explain pipelining instruction sequence in ARM9 and ARM10 ? **[7M]**
b. What instructions are loaded from exception vector table when exceptions or interrupt occurs ? **[7M]**

SECTION-II

3 Explain in detail data processing instruction with example? **[14M]**

OR

4 Describe program status register instructions in detail ? **[14M]**

SECTION-III

5 Write atleast 14 thumb instruction set ? **[14M]**

OR

6 Explain stack instructions and software interrupt instructions with example? **[14M]**

SECTION-IV

7 a. Explain function calls in ARM? **[7M]**

b. What are the rules to generate structure with elements packed for maximum efficiency? **[7M]**

OR

8 Explain in detail register allocation in ARM ? **[14M]**

SECTION-V

9 Explain page tables and translation in detail? **[14M]**

OR

10 c. Explain the basic architecture of cache? **[4M]**

d. Explain the basic operation of cache controller?

e. Draw the diagram of 4 KB cache? **[4M]**

f. How to calculate the cache efficiency? **[4M]**

[2M]

****

Code No: R15D9303

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018

Embedded System Design

(VLSI& ES, & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

*** * * * * ***

SECTION - I

1. (a) Explain the register organization of the ARM processor. (7M)
   (b) Write the various stages of instruction pipeline in ARM9. (8M)

(OR)

2. (a) Discuss the data flow in the ARM processor core. (7M)
   (b) Write about important features ARM 7 and ARM 9 family (8M)

SECTION – II

3. (a) Explain the addressing modes of the ARM with suitable examples. (7M)
   (b) Briefly explain the ARM data processing instructions in detail with suitable Examples. (8M)

(OR)

4. (a) What are the unique features of the ARM instruction set? Explain. (7M)
   (b) Mention the importance of the load and store instructions in ARM with an Examples. (8M)

SECTION – III

5. (a) Discuss the software interrupt instructions used in ARM thumb instruction set . (8M)
   (b) Briefly explain usage of the registers in the ARM thumb mode (7M)

(OR)

6. Write the role of the stack operations in ARM thumb mode. (15M)

SECTION – IV

7. Briefly explain the functions, pointers and structures used in ARM c programming. (15M)

(OR)

8. (a) Write a ARM C code to find the numbers of continuous five 1's in given 6 bytes Data.(7M)
   (b) Write a ARM C code to sort 10 bytes stored in an array. (8M)

SECTION – V

9. Briefly explain the cache architecture and polices of the ARM processors. (15M)

(OR)

10. (a) Explain the implementation of the paging concept in ARM. (7M)
    (b) Write the short notes on context switching in ARM (8M)

Code No: R17D9303

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018

Embedded System Design

(VLSI& ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*** * * * * ***

SECTION - I

11. (a) Write about ARM interrupts and vector table in detail. (8M)
    (b) Explain the ARM design philosophy. (6M)

(OR)

12. (a) Draw the CPSR format of ARM and explain with each bit in detail(7M)
    (b) Describe important features of the ARM families.(7M)

SECTION – II

13. (a) Write the conditional branch instructions in ARM and explain. (7M)
    (b) Discuss about the PSR instructions in ARM processor in detail. (7M)

(OR)

14. (a) Explain the load and store instructions in ARM processor. (7M)
    (b) Write the role of the barrel shifter in ARM instruction set and explain instructions related to it.(7M)

SECTION – III

15. (a) Explain how the code density will be improved by using ARM Thumb Instructions? (6M)
    (b) Discuss about the stack and software interrupt instructions in detail. (8M)

(OR)

16. (a) Write about single and multi register load and store instructions. (7M)
    (b) Discuss about the data processing instructions related to Thumb instruction set. (7M)

SECTION – IV

17. (a) Write a ARM C code to find out the factorial of given number. (5M)
    (b) Write about integer and floating point arithmetic instructions with suitable example. (9M)

(OR)

8. Discuss the various Looping constructs with suitable example in each case. (14M)

SECTION – V

9. Discuss about various methods involved in the handling of ARM MMU. (14M)

(OR)

10. (a) Describe the cache polices used in ARM . (7M)
    (b) Write a short note on access permission in ARM. (7M)

* * * * * * * * * *

Code No: **R15D9303** **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

Embedded System Design

(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

******

SECTION-I

1. (a). What is the arm design philosophy? 7M
   (b) Explain about the architecture of arm processor with neat block diagram? 8M

OR

2. (a) Write about the ARM programmer's model? 8M
   (b) Define pipelining and explain about the 3 stage pipelining in ARM in detail? 7M

SECTION-II

3. (a) Write about the Addressing modes in ARM? 8M
   (b) What is the importance of barrel shifter in data path and discuss the instructions related to the barrel shifter? 7M

OR

4. (a) Discuss about the Load and store instructions in ARM with an example? 8M
   (b) Explain about the conditional instructions in ARM with suitable example? 7M

SECTION-III

5. (a) Give details about the branch instructions in ARM? 7M
   (b) Explain about the difference between ARM and thumb instruction set with suitable example? 8M

OR

6. (a) Explain about the Single-Register and Multi Register Load-Store Instructions? 9M
   (b) Write about the software interrupt instructions? 6M

SECTION-IV

7. (a)Write a C program using function call and how is it compiled in ARM? 6M
   (b) Explain about the floating point number handling in ARM? 9M

OR

8. Write about pointer aliasing with an example and how to avoid pointer aliasing 15M

SECTION-V

9. (a) What is a virtual memory and how it works? 9M
   (b) Write short notes on flushing and cache memory? 6M

OR

10. (a) Explain about the ARM MMU? 10M
(b) Write short notes context switch? 5M

****

Code No: R17D9303

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

Embedded System Design

(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

* * * * * *

SECTION - I

18. (a) Explain ARM processor architecture revisions in detail. [7M]
    (b) Why the ARM processor is preferable for most of portable embedded systems? [7M]

(OR)

19. (a) Discuss the data flow in the ARM processor core. [7M]
    (b) Write about important features ARM 7 and ARM 9 family [7M]

SECTION – II

20. (a) Explain the addressing modes of the ARM with suitable examples [7M]
    (b) Discuss how the ARM processor instruction set is different from other processors. [7M]

(OR)

21. (a) What is the role of the conditional instructions in ARM programming [7M]
    (b) Mention the importance of the load and store instructions in ARM with an Examples [7M]

SECTION – III

22. (a) Explain the interrupt instructions in ARM processor. [7M]
    (b) Discuss the usage of the registers in the ARM thumb mode [7M]

(OR)

23. (a) Write the role of the stack operations in ARM thumb mode. [7M]
    (b) Write the important features of the ARM thumb instruction set. [7M]

SECTION – IV

24. Briefly explain the functions, pointers and structures used in ARM c programming. [14M]

(OR)

25. (a) Write a ARM C code to find the largest and smallest numbers in a 10 bytes of Data [7M]
    (b) Write a ARM C code to check given word is prime number or not. [7M]

SECTION – V

26. Briefly explain the cache architecture and polices of the ARM processors. [14M]

(OR)

27. (a) Explain the implementation of the paging concept in ARM [7M]
    (b) Write the short notes on context switching in ARM [7M]

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	CMOS Analog Circuit Design	UNIT –I TO UNIT-V	Philip E. Allen and Douglas R. Holberg	Oxford University Press, International	Second Edition/Indian Edition, 2010.
2	Analysis and Design of Analog Integrated Circuits-	UNIT -I: MOS Devices and Modeling UNIT -II: Analog CMOS Sub-Circuits	Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer,	Wiley India	Fifth Edition, 2010.
3	Analog Integrated Circuit Design	UNIT -II: Analog CMOS Sub-Circuits UNIT -III: CMOS Amplifiers UNIT -IV: CMOS Operational Amplifiers	David A. Johns, Ken Martin	Wiley Student Edn,	2013

Code No: **R15D6805**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Analog Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

*****

SECTION-I

1 **(a)** Explain about MOS large- signal analysis of CMOS Device Modeling **[10M]**
(b) Explain sub-threshold MOS model Parameters. **[5M]**

OR

2 **(a)** Discuss about the passive components of the MOS transistor. **[7M]**
(b) Write about computer simulation models for MOS transistor **[8M]**

SECTION-II

3 a) Explain the working of current mirror with beta helper **[10M]**
b) Explain the operation of MOS Diode **[5M]**

OR

4 Discuss the Cascode current Mirror and Wilson Current Mirror **[15M]**

SECTION-III

5	(a)Explain about working of differential amplifier	**[10M]**
	(b)Explain the operation of CMOS inverter	**[5M]**

OR

6	Discuss the principle of High Gain Amplifiers Architectures	**[15M]**

SECTION-IV

7	Discuss the concept of op amp compensation and give the necessary expressions.	**[15M]**

OR

8	(a)Explain the Design of Two-Stage Op Amps	**[10M]**
	(b)What are the various measurements of op amp?	**[5M]**

SECTION-V

9	(a) Explain the Discrete-Time Comparators.	**[7M]**
	(b) What is a comparator and list the important characteristics of a comparator	**[8M]**

OR

10	What are the various forms of improving the slew-rate of a 2-stage op amp and obtain the expression for slew rate of CMOS op amp	**[15M]**

****

Code No: R17D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

R17

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION-I

Q.No. 1.a. Draw the physical structure of n channel and p channel MOS transistor using well technology and highlight the importance points? [7M]

b. Explain the importance of BSIM3 model addresses threshold voltage reduction? [7M]

OR

Q.No 2.a. Explain the small signal model for the MOS transistor? [7M]

b. Explain about CMOS device model? [7M]

SECTION-II

Q.No.3.a. Explain the the feedback through effects by using a dummy transistor? [7M]

b.Draw the current sink circuits and explain the VI characteristics? [7M]

OR

Q.No.4.a. What do you mean by band gap reference and list the principle involved? [7M]

b.Draw the circuit diagram of standard cascode current sink and how its reduces the errors in V or I? [7M]

SECTION-III

Q.No.5.a. Draw the circuit diagram of output amplifier using push pull inverting amplifier and comment on it? [7M]

b. Explain the noise model of a p channel differential amplifier ? [7M]

OR

Q.No.6.a. Explain the design relationships for the differential amplifier? [7M]

b. Draw the circuit diagram of differential mode and common mode circuits using CMOS and explain? [7M]

SECTION-IV

Q.No.7. What is compensation of Op-amp? Explain the operation of Miller compensation. [14M]

OR

Q.No.8.a. Explain the design procedure for the 2 stage CMOS opamp? [7M]

b.Explain folded cascode op amp? [7M]

SECTION-V

Q.No.9.a. Explain regenerative comparators? [7M]

b. Draw the switched capacitor comparator and highlight four important points? [7M]

OR

Q.No.10.a. How to improve the performance of an open loop high gain comparator by auto zeroing? [7M]

b. Explain clamped push pull output comparator? [7M]

****

R15

Code No: R15D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

CMOS Analog Integrated Circuit Design
(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

***

SECTION-I

1 a) Draw the large-signal analysis of differential amplifier. **[8M]**
b) Write about Passive Components- Capacitor & Resistor. **[7M]**

OR

2 a)Explain MOS small- signal analysis of CMOS Device Modeling. **[10M]**
b) Draw the circuit diagram for MOS Transistor. **[5M]**

SECTION-II

3 a)Explain the Current Sinks and Sources with Beta Helper. **[10M]**
b) How a MOS transistor acts as switch? **[5M]**

OR

4 a) Discuss the Current and Voltage References with moderate temperature **[10M]**
stability. **[5M]**

b) Explain the operation of MOS Active Resistor.

SECTION-III

5	a) Explain the characteristics of current amplifiers. b) Explain the principle of Output Amplifiers.	**[8M]** **[7M]**

OR

6	Discuss the design features of fully folded cascade op amp.	**[15M]**

SECTION-IV

7	a)Explain about various op amp compensation techniques.	**[8M]**
	b)Draw the internal block diagram of op-amp and explain about each block.	**[7M]**

OR

8	Explain the Power-Supply Rejection Ratio of Two-Stage Op Amps.	**[15M]**

SECTION-V

9	a)Explain different types of comparators with neat circuit diagrams.	**[10M]**
	b) With neat diagram explain Open-Loop Comparators.	**[5M]**

OR

10	Discuss the tradeoffs involved in selecting the input stage as p-channel or channelwith respect to a two stage OP amp.	**[15M]**

****

Code No: R18D6808

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

CMOS Analog Integrated Circuit Design

(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION-I

Q.No 1.a List out the major steps in the design process of a IC and list out the advantages of simulation? [7M]

b. What is sub threshold and its trans conductance characteristics of MOSFET? [7M]

OR

Q.No 2.a In analog process, list the three types of capacitors and draw the capacitor with different polysilicons? [7M]

b. List the dependence of the small signal model parameters on the dc values of voltage and current in the saturation? [7M]

SECTION-II

Q.No 3.a How a MOS diode can be obtained by using MOS transistor, draw the equivalent small signal model? [7M]

b. How to achieve the near zero temperature coefficient by using CMOS? [7M]

OR

Q.No 4.a Draw the circuit diagram of n channel current mirror and the effects of input and out put currents? [7M]

b. Draw the circuit diagram of pn junction voltage reference and how it provides better voltage reference? [7M]

SECTION-III

Q.No.5.a List out the various circuits of inverting CMOs amplifiers and compare? [7M]

b. Explain current mirror differential input current amplifier? [7M]

OR

Q.No.6.a. Explain the large signal voltage transfer curve of the cascode amplifier? [7M]

b.Draw the circuit diagram of CMOS differential amplifier using NMOS transistors and explain? [7M]

SECTION-IV

Q.No. 7.a. Explain the transient response of an op-amp with feedback? [7M]

b. List the categorization and hierarchy of amplifiers based on voltage and current conversions? [7M]

OR

Q.No.8.a. Explain miller compensation of the 2 stage opamp? [7M]

b.What do you mean by PSRR and explain a method for calculating PSRR? [7M]

SECTION-V

Q.No.9.a. Compare four major points of a comparator in static and dynamic characteristics? [7M]

b.Explain the performance of 2 stage uncompensated opamp that can be used a comparator? [7M]

OR

Q.No.10.a. How to improve the performance of an open loop high gain comparator by bistable circuit? [7M]

b. Explain the design of 2 stage open loop comparator? [7M]

****

Code No: R15D6805

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018

CMOS Analog Integrated Circuit Design

(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section-I

1. a. Draw the Large-signal model for the MOS Transistor and explain. 8M
   b. Explain about computer simulation model.7M

OR

2.a Discuss about the Passive Components of the MOS transistor. 8M

b. Draw the small-signal model for the MOS transistor and explain. 7M

Section-II

3.a Draw the given simplest forms of the current mirror for the following i) Bipolar version of current mirror ii) MOS version of the current mirror. 8M

b. Discuss the influence of the capacitance in MOS switch.7M

OR

4.a Draw the circuit diagram of MOSFET switch and discuss the salient features? 8M

b.Discuss the effects on characterization of MOSFET Sinks and Sources. 7M

Section-III

5.a What are the Characteristics of an amplifier and name the types of amplifiers, enumerate the input and output resistances. 8M

b. Design of a CMOS Differential amplifier with a Current Mirror Load ? 7M

OR

6.a Draw the circuit diagram of voltage driven cascode amplifier also discuss Large-Signal Characteristics of the Cascode Amplifier. 8M

b. Briefly explain the differential amplifiers. 7M

Section-IV

7.Explain about the design of Two-stage op-amps and the key design issues of it?15M

OR

8.Explain the various Measurement technologies of Op-amp. 15M

Section-V

9.a.What is a comparator and types and static characteristic of a comparator? 8M

b. Compare infinite and finite gain comparator. 7M

OR

10.a.Draw the Two-Stage Comparator with Increased Speed and write the salient features. 8M

b. Draw the circuit diagram of folded cascade comparator? 7M

****

Code No: R15D6805

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

R15

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

SECTION-I

1.a What do you mean by sub threshold MOS model, explain? [8M]

b. Draw the small-signal model for the MOS transistor. Briefly explain each component in that? [7M]

OR

2. a.Name the types of resistors and capacitors in analog design for CMOS VLSI systems and the factors effecting accuracy? [8M]

b. Explain the Large-signal model for the MOS Transistor. [7M]

SECTION-II

3.a Discuss the influence of the ON resistance in MOS switch. [8M]

b. Explain in details the MOS cascode current mirror with necessary equations. [7M]

OR

4.a Write the analytical expressions to approximate charge injection/clock feed through. [8M]

b. Explain about the Bipolar simple current mirror with degeneration helper with necessary equation.

[7M]

SECTION-III

5.a Draw the circuit diagram of the noise model of inverting amplifiers and summarize the voltage gain and output resistance under various loads. [8M]

b. Explain the Voltage Transfer Characteristic of the Differential Amplifier with current mirror load?

[7M]

OR

6.a Draw the circuit diagram of voltage driven common gate amplifier also discuss Small Signal Performance of the Common Gate Amplifier. [8M]

b. What are the Characteristics of an amplifier and Name the types of amplifiers. [7M]

SECTION-IV

7. Explain the PSRR of the two-stage, Miller compensated op amp? [15M]

OR

8. What are the various cascode schemes of CMOS Op-amps and explain any one? [15M]

SECTION-V

9.a. What is a comparator and types and static characteristic of a comparator? [8M]

b. Compare infinite and finite gain comparator. [7M]

OR

10a. Draw the circuit diagram of two pole comparator and write the salient features. [8M]

b. Draw the circuit diagram of folded cascade comparator? [7M]

****

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Digital Integrated Circuit Design	UNIT –I: MOS Design	Ken Martin	Oxford University Press	2011
2	Digital Integrated Circuit Design	UNIT –II: Combinational MOS Logic Circuits	Ken Martin	Oxford University Press	2011
3	Digital Integrated Circuit Design	UNIT –III: Sequential MOS Logic Circuits	Ken Martin	Oxford University Press	2011
4	CMOS Digital Integrated Circuits Analysis and Design	UNIT –IV: Dynamic Logic Circuits	Sung-Mo Kang, Yusuf Leblebici	TMH	3 rd Ed., 2011
5	CMOS Digital Integrated Circuits Analysis and Design	UNIT –V: Semiconductor Memories	Sung-Mo Kang, Yusuf Leblebici	TMH	23 rd Ed., 011

Code No: R15D6807

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M. Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Digital Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

SECTION-I

1 a) Determine Pull up to Pull down ratio for an NMOS Inverter? **[8M]**
b) How MOS inverters connected in cascade can drive large capacitive loads? **[7M]**

OR

2 a) What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics? **[8M]**
b) Write a short notes on Pseudo NMOS logic gate? **[7M]**

SECTION-II

3 a) Explain and derive necessary DC region equations of CMOS inverter? **[10M]**
b) Consider a CMOS inverter circuit with following parameters: V_{DD}=3.3V,$V_{TO.N}$=0.6V,$V_{TO.P}$=-0.7V,K_N=200uA/V^2,K_P=80uA/V^2.Calculate noise margins of circuit. **[5M]**

OR

4 a) Draw and Explain Voltage transfer characteristics of CMOS inverter with relevant expressions? **[10M]**
b) Explain 2 Input NOR gate with depletion NMOS loads. Calculate output high voltage and output low voltage? **[5M]**

SECTION-III

5 a) Explain Pseudo NMOS implementation of OAI gate **[10M]**
b) Explain the behaviour of the two inverter basic bistable element **5M]**

OR

6 a) Design a CMOS Full adder and Explain its operation using input and output waveforms **[8M]**
b) Explain how the implementations of AOI and OAI Complex CMOS gate topologies are different. **[7M]**

SECTION-IV

7 a**)** Explain dynamic CMOS transmission gate logic? **[8M]**
b) Explain the benefit of Domino CMOS? **[7M]**

OR

8 Explain dynamic circuit technique for overcoming threshold voltage drops in digital circuits **[15M]**

SECTION-V

9 a) Draw the circuit diagram of Dual Port Static RAM and explain its operation. **[10M]**
b) Classify different types of memories in market. **[5M]**

OR

10 a) Draw the functional diagram of 256-Mb Synchronous DRAM and explain all the signals. **[10M]**
b) What are the advantages and disadvantages of DRAM over SRAM **[5M]**

*****

Code No: **R17D6807**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Regular/Supplementary Examinations, Dec-18/Jan 19

CMOS Digital Integrated Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

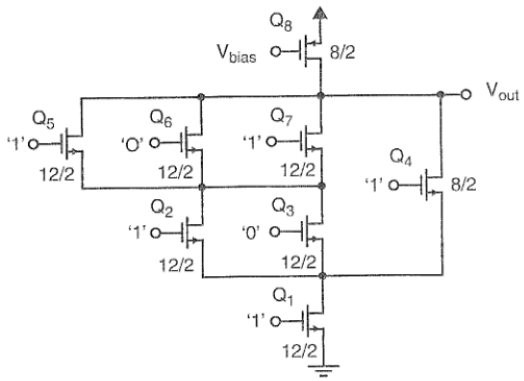
***

SECTION - I

1. a) Draw the circuit diagram of a Pseudo NMOS inverter and CMOS inverter and compare them 7M
   b) Realize the logic circuit of an ex-or gate using Pseudo NMOS logic 7M

OR

2. a) Derive the inverter switching threshold voltage, output high voltage and output low voltage of a pseudo NMOS inverter 7M
   b) Replace the pull down network (in the circuit shown) by a single equivalent transistor 7M



SECTION – II

3. a) Draw the circuit diagram of a 2-input NAND gate with NMOS load and derive its output low voltage. 7M
   b) Sketch the CMOS circuit (with both pullup and pull down network) for realizing the Boolean expression 7M

$$Z' = A(D+E) + BC$$

OR

4. a) Draw the circuit diagram of a 2-input CMOS NOR gate and its sample layout (indicating all the layers and their annotation clearly) 7M
   b) Sketch the complementary pass transistor logic implementation of a NAND2 and NOR2 gate 7M

SECTION – III

5. a) Describe the electrical behavior of bistable element and its potential applications 7M

	b)	Sketch the block diagram, gate level schematic and CMOS implementation of a D-Latch. Also explain its operation	7M

OR

6.	a)	Draw the block diagram, gate level schematic, CMOS schematic and truth table of SR Latch using NOR2 gates	7M
	b)	Draw the block diagram, gate level schematic, AOI NAND-based implementation of clocked SR latch and explain its operation	7M

SECTION – IV

7.	a)	Distinguish between static logic gates and dynamic logic gates with an example	7M
	b)	Describe the cascading problem in dynamic logic gates (with neat circuit diagrams) and suggest a solution	7M

OR

8.	a)	With a neat sketch explain the operation of a voltage bootstrapping circuit	7M
	b)	Explain in detail about dynamic CMOS circuit techniques.	7M

SECTION – V

9.	a)	Classify semiconductor memories and distinguish between SRAM and DRAM memories	7M
	b)	Draw the circuit diagram and explain the operation of a 1-bit SRAM cell in both read and write modes	7M

OR

10.	a)	Draw the circuit diagram of a4-bit X 4-bit NOR based RAM array and explain the operation with its truth table	7M
	b)	With a neat sketch explain the operation of a three transistor 1-bit DRAM cell	7M

****

R15

Code No: R15D6807

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

CMOS Digital Integrated Circuit Design

(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

SECTION-I

1	Explain the concept of resistive load inverter. Calculate output high voltage and output low voltage?	**[15M]**
	OR	
2	Explain the following: a)Enhancement load NMOS inverter b)Depletion load NMOS inverter	**[15M]**

SECTION-II

3	a)Realize one-bit CMOS full adder. b)Explain NAND structure with multiple input and transient analysis of NAND gate?	**[7M+8M]**
	OR	
4	Design a CMOS circuit for Boolean expression $Z=(A(D+E)+BC)'$?	**[15M]**

SECTION-III

5	a)Design clocked NOR-based SR latch circuit using AOI gates ? b)Implement CMOS Negative Edge Triggered Master Slave D Flip-Flop using Transmission gates.	**[8M+7M]**
	OR	
6	a)Explain Operational modes of the transistors in the NOR-based CMOS SR latch circuit b)Draw the gate level, circuit diagram and truth table of the JK latch and explain its operation.	**[8M+7M]**

SECTION-IV

7	Explain multiple-output domino CMOS gate realization using any four functions	**[15M]**
	OR	
8	Explain Cascading domino CMOS logic gates with static CMOS logic gates.	**[15M]**

SECTION-V

9	Explain Flash NAND memory with relevant circuit diagram..	**[15M]**
	OR	
10	a)Draw the circuit diagram of Dual Port Static RAM and explain its operation b)Explain the 1-Bit DRAM Cell operation with a neat diagram	**[8M+7M]**

***

Code No: **R18D6810**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

CMOS Digital Integrated Circuit Design

(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

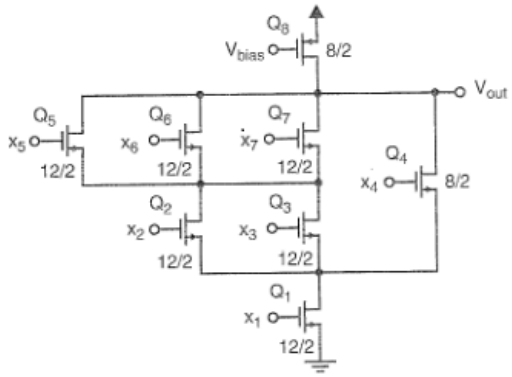
Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION - I

1. a) Draw the circuit diagram of a Pseudo NMOS inverter and derive its inverter switching threshold and output low voltage [7M]

   b) Identify the Boolean expression realized by the shown MOS circuit. Also draw its logic diagram using basic gates [7M]



OR

2. a) Derive the rise time and fall time of a pseudo NMOS inverter [7M]

   b) Draw the circuit diagram of a CMOS inverter and explain its advantages over Pseudo NMOS inverter [7M]

SECTION – II

3. a) Draw the circuit diagram of a gate with output F = [A(B+C)]' with NMOS load [7M]

   b) Draw the circuit diagram of a 2-input CMOS NOR gate and its sample layout (indicating all the layers and their annotation clearly) [7M]

OR

4. a) Draw the circuit diagram of a 2-input CMOS NAND gate and derive its switching threshold [7M]

   b) Sketch the CMOS transmission gate implementation of 2-input XOR gate and 2X1 multiplexer [7M]

SECTION – III

5. a) Sketch the CMOS schematic of a SR latch using NOR2 gates and tabulate the operating modes of the transistors for various input levels [7M]

   b) Draw the block diagram, gate level schematic of clocked SR latch and explain its operation [7M]

OR

6. a) Draw the block diagram, gate level schematic, NMOS load based schematic and truth table of SR Latch using NAND2 gates [7M]

b) Sketch the block diagram, gate level schematic and CMOS implementation of a negative edge triggered D-Flip Flop. Also explain its operation [7M]

SECTION – IV

7. a) Draw the circuit diagram and explain the operation of a dynamic D-Latch [7M]
   b) Explain the charge storage and leakage issues in dynamic logic gates [7M]

OR

8. a) With the help of an example, explain the operation of a domino logic gate [7M]
   b) Write short notes on dynamic cmos transmission gate circuits(with an example) and compare with static CMOS transmission gates [7M]

SECTION – V

9. a) Explain the organization and operation of a random access memory array [7M]
   b) Describe the leakage effects in DRAM cells and explain the operation of the refreshing circuitry. [7M]

OR

10. a) Draw the circuit diagram of a 4-bit X 4-bit NAND based RAM array and explain the operation with its truth table [7M]
    b) Write short notes on flash memories [7M]

***

Code No: R15D6807

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018

CMOS Digital Integrated Circuit Design

(VLSI& ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section-I

1. a. What do you mean by transistor equivalency and explain how it is useful in design of MOS circuits.
(7M)

b. What are the features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate?

(8M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (8M)

b. Explain and derive the necessary DC region equations of a CMOS inverter. (7M)

Section-II

3. a. Explain the procedure to design an adder circuit using CMOS logic. (8M)

b. Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram. (7M)

OR

4.a How the MOS inverters connected in cascade can drive large capacitive loads? Explain. (8M)

b. Write short notes on transmission gates with the relevant circuits. (7M)

Section-III

5.a. Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table. (8M)

b. Differentiate between static and dynamic latches. (7M)

OR

6.a Draw the circuit diagram of CMOS negative edge trigged master slave D FF and explain the features? (8M)

b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

Section-IV

7. a. Explain dynamic boot strapping. (8M)

b. Explain the speed and power dissipation in dynamic CMOS logic.(7M)

OR

8.a. What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch. (8M)

b. What is a dynamic gate and discuss its properties. (7M)

Section-V

9.a What are the types of DRAM? Explain any one. (8M)

b. Describe the leakage currents in DRAM cell. (7M)

OR

10.)a. Compare the SRAM and DRAM. (8M)

b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

Code No: R17D6807

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester supplementary Examinations, Jan/Feb 2018

CMOS Digital Integrated Circuit Design

(VLSI& ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section-I

1. a. What do you mean by transistor equivalency and explain how it is useful in design of MOS circuits. (7M)

b. What are the features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate? (7M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (7M)

b. Explain and derive the necessary DC region equations of a CMOS inverter. (7M)

Section-II

3. a. Explain the procedure to design an adder circuit using CMOS logic. (7M)

b. Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram. (7M)

OR

4.a How the MOS inverters connected in cascade can drive large capacitive loads? Explain. (7M)

b. Write short notes on transmission gates with the relevant circuits. (7M)

Section-III

5.a. Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table. (7M)

b. Differentiate between static and dynamic latches. (7M)

OR

6.a Draw the circuit diagram of CMOS negative edge trigged master slave D FF and explain the features? (7M)

b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

Section-IV

7. a. Explain dynamic boot strapping. (7M)

b. Explain the speed and power dissipation in dynamic CMOS logic.(7M)

OR

8.a. What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch. (7M)

b. What is a dynamic gate and discuss its properties. (7M)

Section-V

9.a What are the types of DRAM? Explain any one. (7M)

b. Describe the leakage currents in DRAM cell. (7M)

OR

10.)a. Compare the SRAM and DRAM. (7M)

b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

Code No: **R15D6807** **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

CMOS Digital Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

******

SECTION-I

1.a Explain the DC noise margin of CMOS logic. (8M)

b. Explain the factors to be considered while choosing transistor sizes? (7M)

OR

2.a Determine the pull-up to pull-down ratio for an NMOS inverter. (8M)

b. What are the Features of pseudo-NMOS logic and draw the circuit diagram of pseudo-NMOS XOR gate?

(7M)

SECTION-II

3.a. Bring out the differences between Pass Transistor logic and transmission gate logic. (8M)

b. Explain the propagation delay and power consumption issues of CMOS gate. (7M)

OR

4. a Design and explain the operation of 2 input NMOS NAND. (8M)

b. Draw the CMOS full adder circuit and explain its operation. (7M)

SECTION-III

5.a Discuss the CMOS two inverter bistable element? (8M)

b. What is the drawback of SR latch and it can be overcome by using feedbacks, draw the circuit diagram of CMOS AOI based JK latch? (7M)

OR

6.a Draw the circuit diagram of Schmitt trigger circuit and explain its operation? (8M)

b. Draw the circuit diagram of CMOS SR latch using NOR gates and operating modes? (7M)

SECTION-IV

7. a. Explain dynamic boot strapping. (8M)

b. Explain the speed and power dissipation in dynamic CMOS logic. (7M)

OR

8.a. What is cascading problem in dynamic CMOS logic and it can be overcome? (8M)

b. Discuss NORA CMOS logic circuit with an example? (7M)

SECTION-V

9.a Write about the leakage currents in SRAM. (8M)

b Explain NOR flash memory? (7M)

OR

10.a Compare the SRAM and DRAM. (8M)

b Write notes on Ferro electric Random Access Memory (FRAM). (7M)

R17

Code No: **R17DME51**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, June 2019

Non Conventional Energy Sources

(MD, TE, VLSI&ES & ASP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

SECTION-I

Q.No. 1 Explain with neat sketch the potential of Renewable energy sources in India. [14M]

OR

Q.No. 2 a) Explain with a neat sketch, the working of solar PV-Power generation. [9M]

b) Write short note on solar still. [5M]

SECTION-II

Q.No.3 Explain with a neat sketch, working of geo thermal power plant for power generation. [14M]

OR

Q.No. 4 a) What are the environmental impacts of geothermal energy? [7M]

b) What are the merits and demerits of geothermal energy? [7M]

SECTION-III

Q.No. 5 a) Explain with a neat sketch about nuclear fusion. [7M]

b) Explain with a neat sketch about nuclear fission. [7M]

OR

Q.No. 6 a) What are the advantages and dis-advantages of the usages of Hydrogen gas as IC Engine fuel? [7M]

b) What are the properties of Hydrogen gas? [7M]

SECTION-IV

Q.No.7 Explain with neat sketch the working of KVIC (Khadi Village Industries Commission) Bio-gas plant. [14M]

OR

Q.No. 8 With a neat sketch explain about fixed dome of movable drum type Bio-gas plant. [14M]

SECTION-V

Q.No. 9 Explain with neat sketches the various types of wind energy turbines.[14M]

OR

Q.No.10 a) What are the Advantages and limitations of wave energy conversion.[7M]

b) State the basic principle of tidal energy production. [7M]

****

Code No: R17DEC51

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular Examinations, Jan/Feb 2018

Embedded Systems Programming

(VLSI& ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION-I

1. Explain the use of semaphore in LINUX operating system with an example(14M)

(OR)

2. Explain the memory management in LINUX operating ssytem. (14M)

SECTION-II

3. Define RTOS? Explain Hard and soft real time system (14M)

(OR)

4. a) Explain the differences between general purpose operating system and RTOS(7M)
   b) What are the disadvantages of RTOS? (7M)

SECTION-III

5. Explain basic issues in selecting a RTOS? Explain.(14M)

(OR)

6. Explain the interprocess communications in RTOS. (14M)

SECTION-IV

7. What is Shared data problem? Explain with an example how semaphore used to solve the problem(14M)

(OR)

8. What are device drivers? Explain device drivers functions in RTOS(14M)

SECTION-V

9. Explain the build process for the embedded systems. (14M).

(OR)

10. Explain different laboratory tools used to test embedded boards(14M)

******

Code No: R17DEC51

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Supplementary Examinations, July/Aug 2018

Embedded Systems Programming

(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

******

SECTION-I

1. Explain in detail file management in LINUX operating system (14M)

(OR)

2. Explain the interfacing of USB device drivers to LINUX operating system (14M)

SECTION-II

3. What is an Interrupt? Explain interrupt routine in RTOS Environment (14M)

(OR)

4. a) Explain the architecture of an RTOS(8M)
   b) What are the advantages of RTOS? (6M)

SECTION-III

5. What is a POSIX standard in RTOS? Explain.(14M)

(OR)

6. Explain Xenomai basics (14M)

SECTION-IV

7. What is a Task in RTOS? Explain Message Queue in RTOS(14M)

(OR)

8. Write short notes on Pipes and signals (7+7=14M)

SECTION-V

9. Explain Tool chain for building embedded software (14M).

(OR)

10. Explain the porting of RTOS to a target board.(14M)

****

COURSE COVERAGE SUMMARY & QUESTION BANK-SEMESTER-II

EMBEDDED REAL TIME OPERATING SYSTEMS

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Advanced UNIX Programming	UNIT – I: Introduction	Richard Stevens		2000
2	Real Time Concepts for Embedded Systems	UNIT - II: Real Time Operating Systems	Qing Li	Elsevier	2011
3	Real Time Concepts for Embedded Systems	III: Objects, Services and I/O IV: Exceptions, Interrupts and Timers V: Case Studies of RTOS	Qing Li	Elsevier	2011

R15

Code No: R15D9314

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, Dec-18/Jan-19

Embedded RTOS

(CSE, VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15marks.

******

SECTION-I

1. a) Write the function of the following: [5*3=15M]
   i)lseek ii) vfork iii) waitpid iv) pend v) fwrite

(OR)

2. a) Write the function of the following: [5*3=15M]
   i)open ii) create iii) close iv) exec v) OSSemPost ( )

SECTION-II

3. a) Why does an OS function provide two modes, user mode and supervisory mode? Briefly explain about those two modes? [8M]
   b) What is the protection mechanism for the OS? Give the various activities for implementing important security functions? [7M]

(OR)

4. a)Discuss about Message Queue States. [7M]
   b)List out various Semaphore Operations . [8M]

SECTION-III

5. How do you create, remove, open, close, read, write and IO control a device using RTOS functions? Take an example of a pipe delivering an IO stream from a network device. [15M]

(OR)

6. a) Explain TCP/IP protocol stack component. [8M]
   b) List out various Pipe Operations? Explain it? [7M]

SECTION-IV

7. a)write about Classification of General Exceptions? [7M]
   b) Give Timer Interrupt Service Routines [8M]

(OR)

8. a) Describe Timing wheel overflow event buffer. [8M]
   b) Soft Timers and Timer Related Operations . [7M]

SECTION-V

9. Discuss the case study of embedded system of mobile phone software for key inputs [15M]

(OR)

10. a) Give the overview of RT Linux. [8M]
    b) Write a program to display a message periodically in RT Linux? [7M]

****

Code No: **R17D9314**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, Dec-18/Jan-19

Embedded Real Time Operating Systems

(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

*****

SECTION-I

Q. No. 1 a)Illustrate the functionalities of any five process control commands in UNIX with relevant examples . [10M]

b) What are the process control in Linx/Unix. [4M]

OR

Q. No. 2 a) What is shared memory ?what are the problems associated with shared memory and explain how they can be overcome? highlight the role of semaphores in RTOS. [7M]

b) Diffrentiate between hard and soft real time systems with relevant examples briefly explain the periodic ,aperiodic and sporadic tasks with examples. [7M]

SECTION-II

Q. No. 3 a)What are the characteristics in RTOS Explain brfiely. [7M]

b) Explain communication and concurrency in RTOS. [7M]

OR

Q. No. 4 a)Explain message queue,states in RTOS. [7M]

b) Explain Synchronization in RTOS. [7M]

SECTION-III

Q. No. 5 a) Explain Objectives and services in RTOS. [7M]

b) Discuss about Pipes and signals in RTOS. [7M]

OR

Q. No.6 a) Explain Remote Procedure Call components with a neat diagram. [7M]

b) What are the building blocks in RTOS explain briefly. [7M]

SECTION-IV

Q. No. 7 a) Explain nested interrupts and stack overflow. [7M]

b) Explain soft timers and timer related operations in detail. [7M]

OR

Q. No. 8 a) Explain all the generic exceptions with examples. [7M]

b) Explain with a neat diagram the programmable interval timers with a system clock initialization. [7M]

SECTION-V

Q. No. 9 a) Explain memory management and processes in Vx Works . [7M]

b) Explain state synchronization of TCP/IP stack tasks in Vx Works. [7M]

OR

Q. No. 10 a) Write a RT-Linux program for controlling a DC motor. [7M]

b) Explain about Rate Monotonic Scheduling and process cycle in detail. [7M]

******

R15

Code No: R15D9314

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
M.Tech I Year - II Semester Supplementary Examinations, June-2019
Embedded RTOS
(CSE, VLSI &ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

****

SECTION-I

1 a)Write the function of the following: **[15M]**
i) lseek ii) vfork iii) wait pid iv) exit v) fwrite
b) Explain about Wrapper function

OR

2 a)Write the functions of the following **[15M]**
i)popen ii)pclose iii)fork iv)exec v)write
b)Write about Unix based real time operating systems

SECTION-II

3 a) What is meant by "Tasks" in RTOS? Explain in detail about task scheduler. **[15M]**
b) Write notes on "Semphares" and "Mutex" in connection with embedded RTOS.

OR

4 Define and briefly explain the following related to embedded RTOS. **[15M]**
a)Message queues
b)Event registers Pipes

SECTION-III

5 a)Explain the building blocks of RTOS with neat sketch **[15M]**
b)Write short notes on port mapped I/O

OR

6 a)Explain Signal control block with neat sketch **[15M]**
b)Draw the pipe state diagram and explain

SECTION-IV

7 a) Explain interrupt service routines related to embedded RTOS. **[15M]**
b) Explain commonly used approaches to real time scheduling

OR

8 a)Explain the Steps in servicing the timer interrupt with suitable diagram **[15M]**
b)Explain Soft Timers and Timer Related Operations

SECTION-V

9 a)Write short notes on RT-Linux threads **[15M]**
b)Explain about Tiny OS kernel design

OR

10 Write short notes **[15M]**
a)MicroC/OS-II
b)Android OS

****

Code No: R18D6804

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Regular Examinations, June-2019

Embedded Real Time Operating Systems

(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	Explain the usage of any 7 commands with example of UNIX/LINUX?	**[14M]**
	OR	
2	Explain with example the Process Control commands of (i) Fork (ii) Vfork (ii) Waitpid (iv) Exec in UNIX/LINUX?	**[14M]**

SECTION-II

3	Define Task and its States & Scheduling, Operation and Structure?	**[14M]**
	OR	
4	Write atleast 4 functional similarities and differences between RTOS and GPOS? Explain about RTOS kernel objects?	**[14M]**

SECTION-III

5	Explain about Pipes and signals.	**[14M]**
	OR	
6	Explain about TCP/IP protocol satck and remote procedure call component?	**[14M]**

SECTION-IV

7	How are Exceptions processed? Difference between ESR and ISR?	**[14M]**
	OR	
8	Explain about Timer Interrupt Service Routines? Define an Exception and Interrupt & Describe its application?	**[14M]**

SECTION-V

9	Explain about Andriod OS?	**[14M]**
	OR	
10	Explain about RT Linux?	**[14M]**

****

Code No: **R15D9314**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018

Embedded RTOS

(CSE, VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

****

Section-I

1. a.what is RTOS ? give on practical example where RTOS is used. (5M)
   b. Write the function of the following (10 M)
   i)lseek ii) vfork iii) waitpid iv) pend v) fwrite

or

2. What is binary semaphore? With an example explain how to use binary semaphores for signaling or notifying occurrences of an event from a task or thread and for signaling or notifying another task waiting for that event. (15M)

Section - II

3. a) Illustrate three examples for specifying hard timing constraints (7M)
   b) Define
   i. Soft Real Time Systems (2M)
   ii. Validation(2M)
   iii. Statistical constraints(2M)
   iv. Hard Real Time Systems(2M)

or

4. a) Explain the memory management that is required for embedded RTOS. (8M)
   b) Write notes on embedded LINUX. (7M)

Section - III

5. a) Differentiate process and thread. (7M)
   b) Define task and explain with diagram all the five states of a task. (8M)

or

6. Define the table for kernel services in an operating system with functions and actions.(15M)

Section - IV

7. a) Explain the creation and activation of a task by task spawn function in Vx Works. (8M)
   b) For task priority function, Define 3 options on spawning. (7M)

or

8. a) Illustrate the block diagram of Automatic Chocolate Vending Machine System(ACVM). (8M)
   b) Explain all the specifications of Hardware architecture of ACVM system. (7M)

Section - V

9. a) Draw and explain the architecture for Air Traffic Control(ATC). (8M)
   b) Illustrate two examples for RTOS Image Processing. (7M)

or

10. (a) Explain the interrupts and Timer interrupt service routines. (7M)
    (b) Explain the purpose of using the real time clock and programmable timers in embedded systems . (8M)

****

Code No: R17D9314

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Regular Examinations, July/Aug 2018

Embedded Real Time Operating Systems

(VLSI &ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

Section-I

Q. No. 1 a) Write a program illustrates the use of fork ( ) function call. [7M]

b) Write short notes on process commands. [7M]

OR

Q. No. 2 a) Explain the goals of services. [7M]

b) Explain the use of Semaphore and write the program. [7M]

Section-II

Q. No. 3 a) Explain the memory management in RTOS . [10M]

b) List the basic design principles in RTOS . [4M]

OR

Q. No. 4 a) Explain the types of RTOS programming. [7M]

b) Explain the system level functions of MicroC/ OS-II in RTOS. [7M]

Section-III

Q. No. 5 a) Draw the basic system of ACVM and explain the system specifications in detail. [7M]

Explain about task and task states with neat diagram. [7M]

OR

Q. No.6 a) Describe about Event Registers. [7M]

b) Explain basic input and out sub systems. [7M]

Section-IV

Q. No. 7 a)Explain the following functional parameters of real time systems. [9M]

i)Pre-emptivity of jobs ii)Criticality of jobs iii)Laxity type and Laxity function

b) Illustrate the weighted round robin approach used in Real time systems with an example and relevant figures

OR

Q. No. 8 a) Interpret the need of RTOS in a Real Time System? List and explain the Important features and services of real time operating systems. [7M]

b) Explain how RTOS can used for implementing the control system applications with examples. [7M]

Section-V

Q. No. 9 a) Draw and explain ACC Hardware Architecture. [7M]

b) Discuss operating system software. [7M]

OR

Q. No. 10 a) Explain the architecture of Android OS. [7M]

b) Discuss OS security issues. [7M]

******

Code No: **R15D9314**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018

Embedded RTOS

(CSE, VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

SECTION-I

6. a) Write the function of the following: [5*3=15M]
   i)lseek ii) vfork iii) waitpid iv) pend v) fwrite

(OR)

7. a) Write the function of the following: [5*3=15M]
   i) open ii) create iii) close iv) exec v) OSSemPost ( )

SECTION-II

8. a) Explain Task and task states? [10M]
   b) List out the various Key Characteristics of an RTOS. [5M]

(OR)

9. a)Discuss about Message Queue. [7M]
   b) Discuss about Scheduling Algorithms. [8M]

SECTION-III

10. How do you create, remove, open, close, read, write and IO control a device using RTOS functions? Take an example of a pipe delivering an IO stream from a network device. [15M]

(OR)

6. a) Explain select operation is allowed on pipes. [8M]
   b) List out various Event Registers? Explain it? [7M]

SECTION-IV

7. a) Nested Exceptions and Stack Overflow?[7M]
   b) Explain Nature of Spurious Interrupts. [8M]

(OR)

8. a) Explain about programmable timers and soft timers. [8M]
   b) Real-Time Clocks and System Clocks. [7M]

SECTION-V

9. Explain how to achieve communication between a process running in Linux and a process running in RTLinux. [15M]

(OR)

10. Explain the case study of coding for sending application layer byte stream on a TCP/IP network using RTOS Vx works. [15M]

******

CMOS MIXED SIGNAL CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Design of Analog CMOS Integrated Circuits-	UNIT -I: Switched Capacitor Circuits	Behzad Razavi	TMH Edition	2002
2	Design of Analog CMOS Integrated Circuits	UNIT -II: Phased Lock Loop (PLL):	Behzad Razavi	TMH Edition	2002
3	CMOS Analog Circuit Design	UNIT -III: Data Converter Fundamentals	Philip E. Allen and Douglas R. Holberg,	Oxford University Press,International	Second Edition/Indian Edition, 2010.
4	Analog Integrated Circuit Design-	UNIT -IV: Nyquist Rate A/D Converters UNIT -V: Oversampling Converters	David A. Johns,Ken Martin,	Wiley Student Edition	2013

Code No: **R15D6811**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018

CMOS Mixed Signal Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

*****

SECTION - I

1. a) Explain the resistor equivalence of a switched capacitor. What is the equivalent resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz? 8M
   b) Describe the different non-ideal effects in switched capacitor circuits 7M

OR

2. a) Draw the circuit diagram of a first-order active RC filter and derive its transfer function. Also derive the corresponding first-order switched capacitor RC filter 8M
   b) With a neat diagram, explain the use of non-overlapping clocks in switched capacitor circuits and mention a possible circuit for clock generation. 7M

SECTION – II

3. a) Explain the operation of a phase detector and describe its input-output characteristics with an example of a possible implementation. Plot the input and output waveforms for a phase difference and frequency difference on the input waveforms 8M
   b) Draw the block diagram of a delay locked loop and explain its operation 7M

OR

4. a) Draw the block diagram of a basic PLL and explain the input-output characteristics of each block. Also draw the waveforms at different points in the system in locked condition 8M
   b) Describe the use of phase locked loops in frequency multiplication and synthesis 7M

SECTION – III

5. a) Describe the deterministic and stochastic modeling of quantization noise in data conversion systems. 8M
   b) What are advantages of reduced resistance ratio based binary scaled converters and explain their operation with neat diagram. 7M

OR

6. a) With a neat circuit diagram, explain the operation of a resistor-string D/A converter and discuss its limitations 8M
   b) With a neat sketch, explain the thermometer code converter and mention its applications 7M

SECTION – IV

7. a) With the help of a flow chart and block diagram, explain the operation of a 8M

successive approximation A/D converter

b) With a neat circuit diagram, explain the operation of a flash A/D converter and discuss the important design issues 7M

OR

8. a) Classify the different A/D converter architectures and comment on their speed, accuracy and basic operating principle 8M

b) Describe the basic principle of interpolating A/D converter and explain its operation with a neat circuit diagram 7M

SECTION – V

9. a) Explain the use of decimation and interpolation filters in oversampling A/D converters 8M

b) Write short notes on the advantages and architecture of higher order modulators in oversampling A/D converters 7M

OR

10. a) With the help of a neat block diagram, describe the system architecture of Delta-Sigma D/A Converters 8M

b) Distinguish between oversampling without and with noise shaping 7M

****

Code No: **R17D6811**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Mixed Signal Circuit Design

(VLS&ES)

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

****

SECTION-I

Q. No. 1 a) Explain briefly about switch sharing [7M]

b) Explain briefly about biquad filters. [7M]

OR

Q. No. 2 a) Explain Basic Building Blocks of Switched Capacitor Circuits. [7M]

b) Explain the characteristics of switched capacitors. [7M]

SECTION-II

Q. No. 3 a) Explain the non-ideal effects in PLLs [6M]

b) Write shot notes on the following

(i) Basic PLL topology (ii) Dynamics of simple PLL [8M]

OR

Q. No. 4 a) what are delay locked loops and explain its operation [9M]

b) Explain Applications of DLL [5M]

SECTION-III

Q. No. 5 a) Explain the operation of decoder based converters [10M]

b) Write shot note Quantization noise [4M]

OR

Q. No.6 a) what are the DC and dynamic specifications of the data converters? [7M]

b) Explain the Hybrid converters [7M]

SECTION-IV

Q. No. 7 a) Find the value of C_1 of a 16-bit integrating A/D converter, having a peak voltage V_X=5v and an input voltage v_{in}=3v.also the converter has an input signal at 50Hz and R_1=100MΏ. [7M]

b) Explain the architecture and working of interpolating ADC. [7M]

OR

Q. No. 8 a).Realize a 4-bit pipelined adder using latches and explain its operation. [10M]

b) Explain the Folding A/D converters. [4M]

SECTION-V

Q. No. 9 a) Explain the Higher order modulators [7M]

b) Explain the Noise shaping modulators [7M]

OR

Q. No. 10 a) Explain the Decimating filters and interpolating filters [14M]

R17

Code No: R17D6811

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, June-2019

CMOS Mixed Signal Circuit Design

(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1 With a neat circuit diagram, explain the resistor implementation of switched capacitor circuit. **[14M]**

OR

2 With a neat circuit diagram, explain the operation of a switched capacitor parasitic sensitive integrator and identify its limitations **[14M]**

SECTION-II

3 Derive the transfer function of a type-I PLL and analyze the various tradeoffs **[14M]**

OR

4 With a neat circuit diagram, explain the operation and applications of Delay locked loops **[14M]**

SECTION-III

5 Define quantization noise and explain its deterministic and stochastic modelling. A sinusoidal signal is applied to an ideal 12-bit A/D converter for which $V_{ref} = 5$ V. Find the SNR of the digitized output signal. **[14M]**

OR

6 Deign a Thermometer code charge redistribution D/A converter. **[14M]**

SECTION-IV

7 What is flash converter? Discuss the working of a 3 bit flash A/D converter **[14M]**

OR

8 What is time interleaving? Explain the operation of a time interleaved ADC **[14M]**

SECTION-V

9 Explain the block diagram of second order Delta-Sigma modulator **[14M]**

OR

10 With a neat block diagram, explain the system architecture of Delta-Sigma D/A Converters **[14M]**

Code No: R15D6811

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester supplementary Examinations, Jan/Feb 2018

CMOS Mixed Signal Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks

******

.Section-I

1. a) Explain the non-ideal characteristics of a switched capacitor integrator. [8M]
   b) Explain the techniques that are adopted in a switched capacitor integrator circuit to minimize charge injection issues. [7M]

OR

2.a) Draw the basic circuit of a switched capacitor, its equivalent circuit , explain its operation and derive its equivalent resistor value. [10 M]
   b) For the above circuit if clock frequency is 100kHz, find the capacitor value that will emulate 1M ohm resistor. [5M]

Section-II

3.a) Explain the basic charge pump PLL and non-ideal effects in PLLs. [8M]
   b) Explain the Jitter in PLLs and delay locked loops. [7 M]

OR

4.a) With the help of necessary waveforms, explain about the non-ideal effects in PLLs. [8M]
   b) Explain about the basic charge pump PLL with a neat figure. [7M]

Section-III

5.a). Explain Binary Scaled converters. [7M]
   b) Write about hybrid converters. [8M]

OR

6.a) Explain about deterministic approach and statistic approach of quantization noise in data converters. [8M]
   b) Design a decoder based DAC with a detailed explanation.[7M]

Section-IV

7.a) Mention all kinds of medium speed and high speed ADC and explain the operation of a multiple- bit pipeline ADC. [8M]
   b) What is a Flash converter? Discuss the working of a 3-bit Flash A/D Converter. [7M]

OR

8.a) Draw the block diagram of a D-A converter in signal processing applications. [8M]
   b) Explain the static and dynamic characteristics of DAC. [7M]

Section-V

9.a) Discuss about Delta-Sigma ADC. [7M]
   b) Explain the block diagram of second order Delta-Sigma modulator. [8 M]

OR

10.a) Design a high-speed noise-shaping converter using a cascaded modulator. [7M]

b) Explain Interpolating Filters and Decimating Filters. [8M]

****

Code No: **R15D6811**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, July/Aug 2018

CMOS Mixed Signal Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

******

SECTION - I

1.	a)	Describe the basic building blocks of switched capacitor circuits and list their desirable characteristics	8M
	b)	What is the equivalent resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz?	7M
		OR	
2.	a)	With the help of a neat circuit diagram, explain the operation of parasitic-sensitive and parasitic-insensitive switched capacitor integrator	8M
	b)	Derive the active RC realization of a continuous time biquad filter with the help of signal flow graph realization.	7M

SECTION – II

3.	a)	Draw the block diagram of a basic PLL and explain the input-output characteristics of each block.	8M
	b)	Explain the use of phase locked loops in clock skew and jitter reduction	7M
		OR	
4.	a)	With the help of neat waveforms, explain the operation of phase-frequency detector and derive a possible implementation	8M
	b)	Derive the transfer function of a Type-I PLL and describe the tradeoffs	7M

SECTION – III

5.	a)	Describe the input-out description of an ideal D/A and A/D converter with appropriate mathematical equations and input-output plots.	8M
	b)	With a neat sketch, explain the thermometer code converter and mention its applications	7M
		OR	
6.	a)	Describe the deterministic and stochastic modeling of quantization noise in data conversion systems.	8M
	b)	Draw the circuit diagram and explain the operation of binary –weighted resistor converters	7M

SECTION – IV

7.	a)	What is the fundamental advantage of a pipelined A/D converter? Explain the signal flow and operation of one bit per stage pipelined converter	8M

	b)	Classify the different A/D converter architectures and comment on their speed and accuracy.	7M

OR

8.	a)	With the help of a flow chart and block diagram, explain the operation of a successive approximation A/D converter	8M
	b)	Explain the issues in the design of flash A/D converter	7M

SECTION – V

9.	a)	With the help of a neat block diagram, describe the system architecture of Delta-Sigma A/D Converters	8M
	b)	Distinguish between oversampling without and with noise shaping	7M

OR

10.	a)	Explain the use of decimation and interpolation filters in oversampling A/D converters	8M
	b)	Derive the switched-capacitor realization of a First-Order A/D Converter .	7M

****

Code No: R17D6811

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Regular Examinations, July/Aug 2018

CMOS Mixed Signal Circuit Design

(VLSI &ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

Section-I

Q. No. 1 What are the basic building blocks of switched capacitors and explain about each of them.[14M]

OR

Q. No. 2 Explain the operation of switched capacitor integrators first order filters. [14M]

Section-II

Q. No. 3 a) List out the various applications of the PPL and explain about any two of them. [8M]

b) Write in detail about the phase/frequency detector. [6M]

OR

Q. No. 4 a) Explain the operation of basic charge pump in PLL? [7M]

b) Explain the operation of Jitter in PLL [7M]

Section-III

Q. No. 5 what are the various Nyquist rate D/A converters and explain in detail about any two of them? [14M]

OR

Q. No.6 a) Explain the operation of binary scaled converters. [7M]

b) Explain the operation of Thermometer-code converters. [7M]

Section-IV

Q. No. 7 a) What is flash converter? Explain its 3 bit flash type A-D converter. [7M]

b) Explain the operation of successive – approximation converters. [7M]

OR

Q. No. 8 a) Discuss the advantages and disadvantages of using a dual slope over a single slope ADC.[7M]

b) Explain the Data Converter Fundamentals. [7M]

Section-V

Q. No. 9 with neat block diagram, describe the operation of multistage decimation filter operation.

[14M]

OR

Q. No. 10 a) Explain the Delta sigma modulators with multibit quantizers. [7M]

b) Explain the principle of interpolation filters**.[7**M]

*****

LOW POWER VLSI DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXTBOOK TITLE	UNITS/TOPICS COVERED	AUTHOR	PUBLISHERS	EDITION
1	Low-Voltage, Low-Power VLSI Subsystems	I,II	Kiat-Seng Yeo, Kaushik Roy	TMH Professional Engineering	TMH
2	Introduction to VLSI Systems: A Logic, Circuit and System Perspective	I,II	Ming-BO Lin	CRC Press	2011
3	CMOS Digital Integrated Circuits – Analysis and Design	III,IV,V	Sung-Mo Kang, Yusuf Leblebici,	TMH	2011

Code No: **R17D6812**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, Dec-18/Jan-19

Lower Power VLSI Design

(VLS&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

****

SECTION-I

Q. No. 1 a) Discuss the need for Low Power circuit design (6M)

b) Can you elaborate on the reasons for Switching Power Dissipation? (8M)

OR

Q. No. 2 a) Define power dissipation and list the sources of Power Dissipation. (4M)

b) Discuss about DIBL and surface scattering. (10M)

SECTION-II

Q. No. 3 a) Explain the basic concepts of supply voltage scaling. (6M)

b) How would you achieve the low power using VTCMOS? (8M)

OR

Q. No. 4 What could be done to minimize the Switched Capacitance? (14M)

SECTION-III

Q. No. 5 a) Write about standard Adder cells that are used for low power circuit design (6M)

b) Can you elaborate the trends of Technology and power supply voltage? (8M)

OR

Q. No.6 Evaluate the performance of different CMOS adders (14M)

SECTION-IV

Q. No. 7 a) Construct and explain the multiplier architecture suitable for signed and unsigned numbers (10M)

b) Write about the classification of multipliers (4M)

OR

Q. No. 8 a) Explain about Braun multiplier with help of neat Schematics (8M)

b) What is the main idea of performance enhancement in Braun multiplier (6M)

SECTION-V

Q. No. 9 a) Write about low power techniques at circuit level while designing a ROM (8M)

b) Briefly write about future trends and developments of ROMs (6M)

OR

Q. No. 10 a) Draw and explain the Pre-charge and Equalization Circuit used in memories (8M)

b) Draw the structure of 6T- SRAM and explain its operation (6M)

Code No: R17D6812 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, June-2019

Low Power VLSI Design

(VLSI & ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	What are the sources of leakage power dissipation and methods to minimize them	**[14M]**
	OR	
2	Write short notes on velocity saturation and Drain Induced barrier lowering	**[14M]**

SECTION-II

3	Describe the use of multi-threshold CMOS circuits for minimization of power dissipation of CMOS circuits	**[14M]**
	OR	
4	Explain the circuit level measures for switched capacitance minimization	**[14M]**

SECTION-III

5	With neat block diagrams/sketches, describe the operation of ripple carry adders and carry look-ahead adders and compare their metrics	**[14M]**
	OR	
6	Explain the different low-power, low-voltage logic styles for minimizing power dissipation	**[14M]**

SECTION-IV

7	With the aid of neat sketches/ diagrams explain in detail about working of baugh-wooley multiplier.	**[14M]**
	OR	
8	Describe the design techniques for low voltage low power multiplier design	**[14M]**

SECTION-V

9	Distinguish between Static RAM and Dynamic RAM. Explain the circuit diagram of dynamic RAM cells and its self-refresh circuit	**[14M]**
	OR	
10	Draw and explain the ROM cell array based on NOR configuration	**[14M]**

****

Code No: R17D6812

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Regular Examinations, July/Aug 2018

Low Power VLSI design

(VLSI &ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

SECTION-I

Q. No. 1 a) What are the various issues involved in low power VLSI Design? Explain (6M)

b) Explain about Sub-threshold leakage in a MOS transistor (8M)

OR

Q. No. 2 What is short channel effect and can you elaborate the short channel effects? (14M)

SECTION-II

Q. No. 3 a) With necessary schematics explain the concept of MTCMOS technique (6M)

b) Can you distinguish between pipelining and parallel processing approaches with suitable examples? (8M)

OR

Q. No. 4 a) How could you minimize the switched capacitance at the system level? (8M)

b) How the low power design can be achieved through Voltage Scaling? (6M)

SECTION-III

Q. No. 5 a) Draw the architecture of Carry look ahead Adder and explain its working (6M)

b) Compare Carry Select and Ripple Carry Adders in terms of delay and area (8M)

OR

Q. No.6 Can you construct and explain the low-voltage low-power Logic Styles (14M)

SECTION-IV

Q. No. 7 Elaborate the operation of Baugh-Wooley multiplier with suitable neat sketches (14M)

OR

Q. No. 8 a) Discuss the modified Booth Recoding technique. (8M)

b) What are the building blocks would you choose for binary array multiplier and explain (6M)

SECTION-V

Q. No. 9 a) Briefly explain about techniques at architecture level used to design low power memories (6M)

b) What way would you design the chip architecture of a 1024-bit ROM and explain its operation (8M)

OR

Q. No. 10 a) Discuss the importance of Self-Refresh circuit and explain any one method. (8M)

b) Explain the read and write operations 1-T DRAM cell (6M)

****

Code No: **R17D9310**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Supplementary Examinations, Dec-18/Jan-19

Adhoc- Wireless Networks

(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

******

SECTION-I

Q. No. 1 a) Compare wireless and wired transmission? [7M]

b) In order to design a adhoc wireless system, explain the major issues and challenges that need to be considered? [7M]

OR

Q. No. 2 a) How the personal devices communicate each other in the absence f infrastructure, explain? [7M]

b) List the types of WLANs, and the components of a typical WLAN? [7M]

SECTION-II

Q. No. 3 a) While designing a MAC protocol for adhoc wireless networks, explain the issues that need to addressed? [7M]

b) Classify and write briefly MAC protocols? [7M]

OR

Q. No. 4 a) Draw the frame format in collision avoidance time allocation protocol and explain its operation? [7M]

b) Illustrate the piggy backing and table update mechanism in distributed priority scheduling in Adhoc networks? [7M]

SECTION-III

Q. No. 5 a) What are the major issues that a routing protocol designed for adhoc wireless networks? [7M]

b) Explain classification of routing protocol? [7M]

OR

Q. No. 6 a)Explain cluster head gateways switch routing protocol with an example? [7M]

b)With an example, explain the route establishment in dynamic source routing protocol? [7M]

SECTION-IV

Q. No. 7 a) Explain the issues to be considered while designing transport layer protocol for adhoc wireless networks? [7M]

b) Explain design goals of transport layer protocol ? [7M]

OR

Q. No. 8 a) Classify and briefly explain any one TCP over adhoc wireless networks protocol? [7M]

b) Explain the operation of TCP-Bu s with an example? [7M]

SECTION-V

Q. No. 9 a) Compare wireless sensor and adhoc wireless networks? [7M]

b) Name the different kinds of sensor network architectures and explain any one? [7M]

OR

Q. No. 10 a) Explain chain based three level scheme? [7M]

b) How the voronoi diagram solves the coverage problem in sensor network? [7M]

****

R18

Code No: R18D6813

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Regular Examinations, June-2019

Adhoc- Wireless Networks

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	Explain Bluetooth architecture and its applications	**[14M]**
	OR	
2	Write about the issues involved Adhoc Wireless Networks	**[14M]**

SECTION-II

3	Explain difference between Contention protocols with reservation system and Contention protocols with scheduling mechanism	**[14M]**
	OR	
4	Explain in detail about the MAC protocols that use Directional antennas and the advantages and disadvantages of it.	**[14M]**

SECTION-III

5	Explain the Classification of Routing Protocols along with any On Demand Routing Protocol	**[14M]**
	OR	
6	What are the various Power – Aware Routing Protocols and explain any one in detail with	**[14M]**

SECTION-IV

7	What are the various Transport Layer protocols available and explain any one in detail	**[14M]**
	OR	
8	Explain the Design issues of the Transport layer Protocol along with the design goals of them	**[14M]**

SECTION-V

9	Explain the sensors network architecture and its applications.	**[14M]**
	OR	
10	How to evaluate the Quality of a sensor network and write about various MAC Protocols of the sensor Network and explain one in detail	**[14M]**

****

Code No: R17D9310

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Regular Examinations, July/Aug 2018

Adhoc-Wireless Networks

(VLSI &ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

SECTION-I

Q. No. 1 a) Write about the design goals of WLANs? [7M]
b) Explain Bluetooth in detail. [7M]

OR

Q. No. 2 a) Explain fundamentals of WLANs'? [7M]
b) Explain the functionalities that the MAC layer provides in IEEE 802.11 WLANs? [7M]

SECTION-II

Q. No. 3 a) While designing a MAC protocol for adhoc wireless networks, explain the issues that needs to addressed? [7M]
b) What are the important goals to be met while designing a MAC protocol for adhoc wireless networks? [7M]

OR

Q. No. 4 a) Draw the frame structure in five phase reservation protocol and explain the phases of the reservation process? [7M]
b) With a diagram, explain the data transmission mechanism in multiple access collision technique? [7M]

SECTION-III

Q. No. 5 a) Broadly classify routing protocols for adhoc wireless networks and briefly explain? [7M]
b) Explain any one hybrid routing protocols with an example [7M]

OR

Q. No. 6 a) With an example, explain the destination sequenced distance vector routing protocol? [7M]
b) With an example, explain the optimized link state routing protocol? [7M]

SECTION-IV

Q. No. 7 a) Name the important goals to be met while designing a transport layer protocol for wireless networks? [7M]
b) Classify and briefly explain transport layer protocol? [7M]

OR

Q. No. 8 a) Explain the issues to be considered while designing transport layer protocol for adhoc wireless networks? [7M]
b) Name the reasons behind through put degradation that TCP faces when used in adhoc wireless networks? [7M]

SECTION-V

Q. No. 9 a) Classify and draw the tree structure of sensor network protocols? [7M]
b) Explain the issues and challenges in designing a sensor network? [7M]

OR

Q. No. 10 a) Explain data dissemination ? [7M]

b) Explain data gathering? [7M]

****

Code No: R18D6818 **R18**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Regular Examinations, June-2019

Multimedia Signal Coding

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 SECTIONs. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION -I

1.a. Identify three novel applications of the Internet or multimedia applications. Discuss why you think these are novel. [7M]

b. How are color models and coordinates systems really used for stored, displayed, and printed images? Explain any one with an example? [7M]

OR

2.Explain in detail different image file formats and image formation with a neat sketch. [14M]

SECTION -II

3.a Classify the types of video signals and explain any two? [7M]

b. Explain quantization and transmission of audios. [7M]

OR

4.a What do you mean by interlacing and explain how it is used in NTSC? [7M]

b.Draw the block diagram of PCM signal encoding and decoding and the importance of each block? [7M]

SECTION-III

5.a Apply shanon fano coding for the word "BOTTO", determine the total number of bits required? [7M]

b. Explain with a block diagram , the compression is achieved? [7M]

OR

6. Explain with a neat block diagram JPEG and hierarchical JPEG. [14M]

SECTION-IV

7.a Explain the basic steps involved in Video Compression algorithms for motion compensation? [7M]

b. Explain MPEG2 video compression standard? [7M]

OR

8.a With the help of a block diagram explain a three-level hierarchical search for motion vectors? [7M]

b. Name the six hierarchical layers for the bit stream of an MPEG-l video sequence with the help of a block diagram? [7M]

SECTION-V

9.a With the help of block diagram explain Channel vocoder? [7M]

b. Explain MPEG-4 Audio standard? [7M]

OR

10.a With the help of block diagram explain CELP analysis model with adaptive and stochastic codebooks? [7M]

b. How an PCM audio signal into coded audio signal is done in MPEG 1 audio layers 1 and 2, explain? [7M]

****

Code No: R18DEC52

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - II Semester Regular Examinations, June-2019

Research Methodology

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	a) Define Research and list out the objectives of Research b) Distinguish between Research Method Vs Research Methodology	**[7M]** **[7M]**
	OR	
2	Briefly Explain the Research approaches with suitable Examples	**[14M]**

SECTION-II

3	Write note on: (a) Review of Literature (b) Null Hypothesis	**[14M]**
	OR	
4	Write note on: (a) Process of identifying Variables (b) Alternative Hypothesis	**[14M]**

SECTION-III

5	Classify research design with suitable examples.	**[14M]**
	OR	
6	(a) Explain the Salient Features of Experimental Research design (b) Distinguish between primary data and secondary data	**[7M]** **[7M]**

SECTION-IV

7	Define Sampling. Explain the probability and non-probability sampling methods	**[14M]**

OR

8 Explain the Correlation and Regression Analysis with suitable Diagrams **[14M]**

SECTION-V

9 What is a research proposal? As a good researcher, state the precautions that you take while writing a business research proposal. **[14M]**

OR

10 Calculate a paired chi-square test for the following data: **[14M]**

Subject #	Score 1
1	3
2	3
3	3
4	12
5	15
6	16
7	17
8	19
9	23
10	24
11	32

****

DESIRE

Education is a progressive discovery of our own ignorance. As knowledge is power, a focus must be given in grooming dynamic leaders, not just graduates. Education is transmission of civilization. Our society needs Enthusiasts with passion to transform India into a "Force to reckon with". I believe that the aim of Education is the knowledge not of facts but of values.

Ch. Malla Reddy

MRCET

A thought beyond horizons of success
committed for Professional Excellence

GLIMPSES OF MRCET

Vision:

- To become a model institution in the fields of Engineering, Technology and Management.
- To have a perfect synchronization of the ideologies of MRCET with challenging demands of International Pioneering Organizations.

Mission:

- To establish a pedestal for the integral innovation, team spirit, originality and competence in the students, expose them to face the global challenges and become pioneers of Indian vision of modern society

MRCET Philosophy:

- To pursue continual improvement of teaching learning process of Undergraduate and Post Graduate programs in Engineering & Management vigorously.
- State of the art infrastructure and expertise to impart the quality education.
- To nurture the students to become emotionally balanced, intellectually creative and professionally competitive.
- Attitude with blend of technology will constitute you to the greatest horizon ever possible.
- To groom the students to become intellectually creative and professionally competitive.

Special Achievements:

- UGC Autonomous Institution, Govt. of India.
- Accredited by NBA, AICTE, New Delhi.
- Accredited by NAAC-A Grade, UGC, Govt. of India.
- Institute has been certified with ISO 9001:2015
- UGC 2f & 12(B) recognized institution, UGC New Delhi
- Research Centre Status, JNTUH, Hydearbad
- MoU with NRDC, Govt. of India.
- MoU with University of New Orleans, USA
- MoU with International Technological University, USA
- MoU with University Malaysia Sarawak (UNIMAS), MALAYSIA
- MoU with ECPI University, USA
- MoU with Lincoln University College, MALAYSIA
- Recognized e.Gov Campus by Engineering Watch, Re-Engineering India.
- MoU with National Aerospace Laboratories (NAL), Bangalore.
- Industry Institute Partnership Cell (IIPC)
- MRCET is a life member of NHRD Network
- CISCO International Certification Authorized Centre.
- MoU with ESOL Examinations (BEC) University of Cambridge, UK.
- Approved to admit Foreign Students/PIO's
- Nodal Center: IIT – Bombay/Kharagpur for Technology Transfer
- Microsoft Innovative Center.
- NASSCOM Nodal Center for NAC-Test Assessment
- JAVA Certification through Oracle Academy
- MoU with Zensar Technologies for the Technology Transfer
- MoU with Tech Mahindra
- Academic Partner – Wipro Technoloiges
- Business Incubation Centre – MSME, Govt. of India
- Global Education and Career Counseling Centre
- Patents award – 4 No's

Principal:
Dr. VSK Reddy
B.Tech, M.Tech, Ph.D (IIT-KGP), FIETE, MIEEE, MISTE, MCSI

Website: www.mrcet.ac.in
EAMCET/PGECET/ICET Code: **MLRD**
Contact: 7207034237, 9133555162